RF On-Chip Filters
Using Q-enhanced LC Filters

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RF On-Chip Filters
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To my beloved family

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SUMMARY

Radio frequency (RF) filters are one of the key building blocks in modern microelectronic digital communication systems that use a narrow frequency band with strong interferers nearby. With the fast advancement of complementary metal oxide (CMOS) fabrication technology, more and more signal-processing functions are implemented in the digital domain for a lower cost, lower power consumption, higher yield, and higher re-configurability. There is always a strong interest in integrating the RF filters on chip with mainstream deep-submicron CMOS technology. But nowadays RF filters still remain one of the few off-chip blocks due to the following main difficulties in integrating RF filters on-chip:

1. High dynamic range (DR) requirement. Since the RF filter is the block right after/before antenna in receiver/tranmitter path, the DR requirement is usually very high (>55 dB). It turns out that the DR requirement is the most important factor to enable RF filters on-chip.

2. The need for automatic tuning circuits. This is probably the second most important factor to enable RF filters on-chip.

3. Low-power requirement. This is typically true especially for mobile application.

4. High common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) requirements.

The objective of this thesis is to explore the better DR performance of RF filters using the Q-enhanced LC filter. It takes a divide-and-conquer method by designing

1. A new simple pseudo-differential pair (PDP) for input g_m stage. It is the fastest, high-linearity, low-distortion, and wide-range constant–g_m design reported to

date. This has been applied in the final filter tape-out and has proven to be effective experimentally.

2. A new tunable discrete inductor (TDL) to achieve two-level inductance with the same real estate that can be used to expand the filtering frequency range. This has been verified experimentally.

3. A new tunable discrete capacitor (TDC) to achieve high linearity over wide terminal voltage swing range. This has been verified through simulation.

4. A new systematic way to achieve synchronized gain, center frequency, and filtering Q tuning capability for Q-enhanced LC filters. It has been verified through simulation.

In order to verify the concept, a 900 MHz filter is designed and fabricated with National Semiconductor Company (NSC)'s standard 0.18 μm digital epi–substrate CMOS technology, and packaged with NSC's LLP-28. The measurement results show that with filter Q of 17 at 845 MHz, the 1 dB compression point is measured to be +4 dBm, IIP3 to be +16 dBm with a peak noise floor of -154 dB/Hz, spurious free dynamic range (SFDR) to be 71 dB. With filter Q of 70 over a 20 MHz BW, the 1 dB compression point is measured to be -9.5 dBm, IIP3 to be +7 dBm with a peak noise floor of -141 dB/Hz, SFDR to be 57 over 20 MHz BW. This filter uses between 56 and 60 mA with a power supply of 1.8 V due to the low-Q (Q$\sim$1) of inductor. It is the RF filter with the highest DR in the published literature. The DR can be even higher if inductor Q can be improved as DR is proportional to Q^2.

CHAPTER 1

INTRODUCTION

1.1 Challenges in integrating RF filters on-chip

In the third quarter of 2002, the Nokia 7210, a cell phone consisting of an ensemble of the newest technologies and leading trends of future cellular phones, was introduced to the European, African, and Asian markets. While its price is comparable to the initial price of the Nokia 8310 phone, it is much more powerful with many more functions added and/or enhanced, as shown in Table 1.

The Nokia 7210 is also a perfect verification of the next-generation wireless system that was predicted just about a year ago [36], as shown in Table 2.

Table 2 shows the technical implications of these trends. With the highest level of integration, the future transceiver will eventually look like what is shown in Figure 1.

Also presented in [16] is an illustrative picture of the current transceiver as shown in Figure 2.

In order to achieve the higher level of integration, first, we can make the whole transceiver monolithic with BiCMOS (SiGe) technology. Power amplifiers (PAs) made from SiGe technology were already reported by IBM in January 2002 [19]. In the future, high-cost, low-yield GaAs will probably be replaced by SiGe that already has a comparable transition frequency (f_T) and better thermal reliability. With the rapid advancement of CMOS fabrication technology, more and more signal-processing functions are implemented in the digital domain for a lower cost, lower power consumption, higher yield, and higher re-configurability. Hence, the cost and size will be further reduced. Second, to further improve transceiver integration, the LC tanks associated

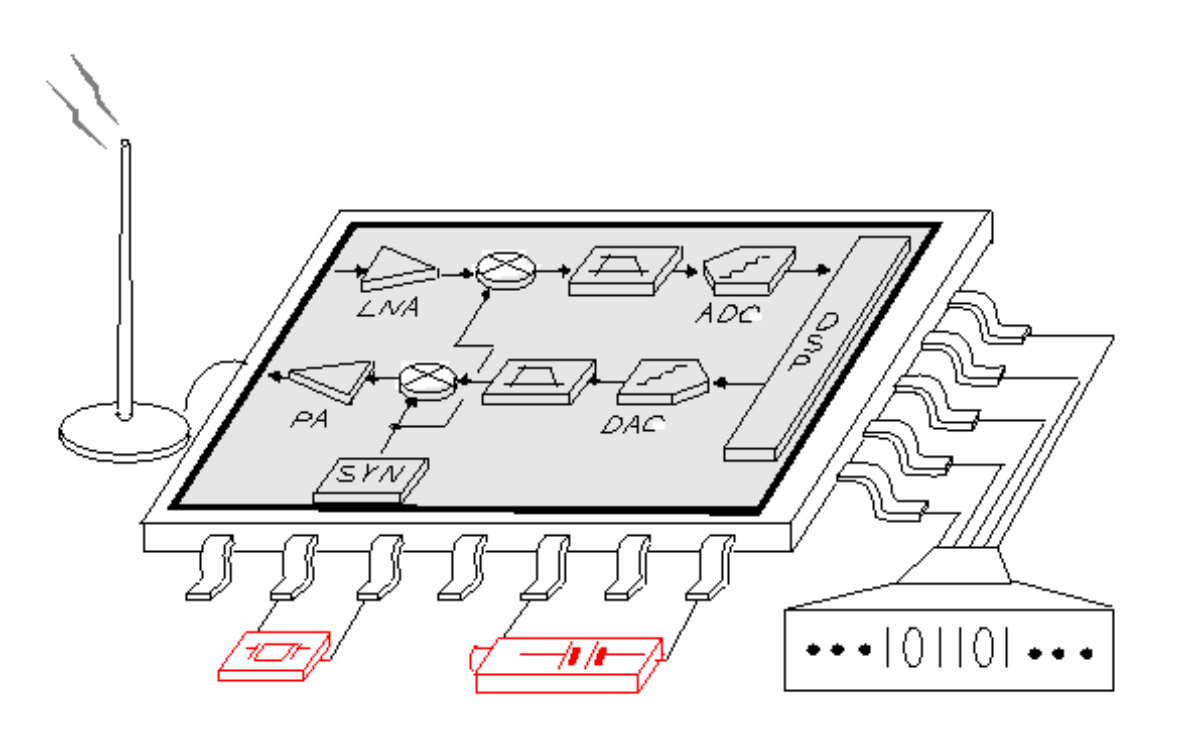


Figure 1: Ultimate single-chip, scaled BiCMOS transceiver with minimum external components [16]

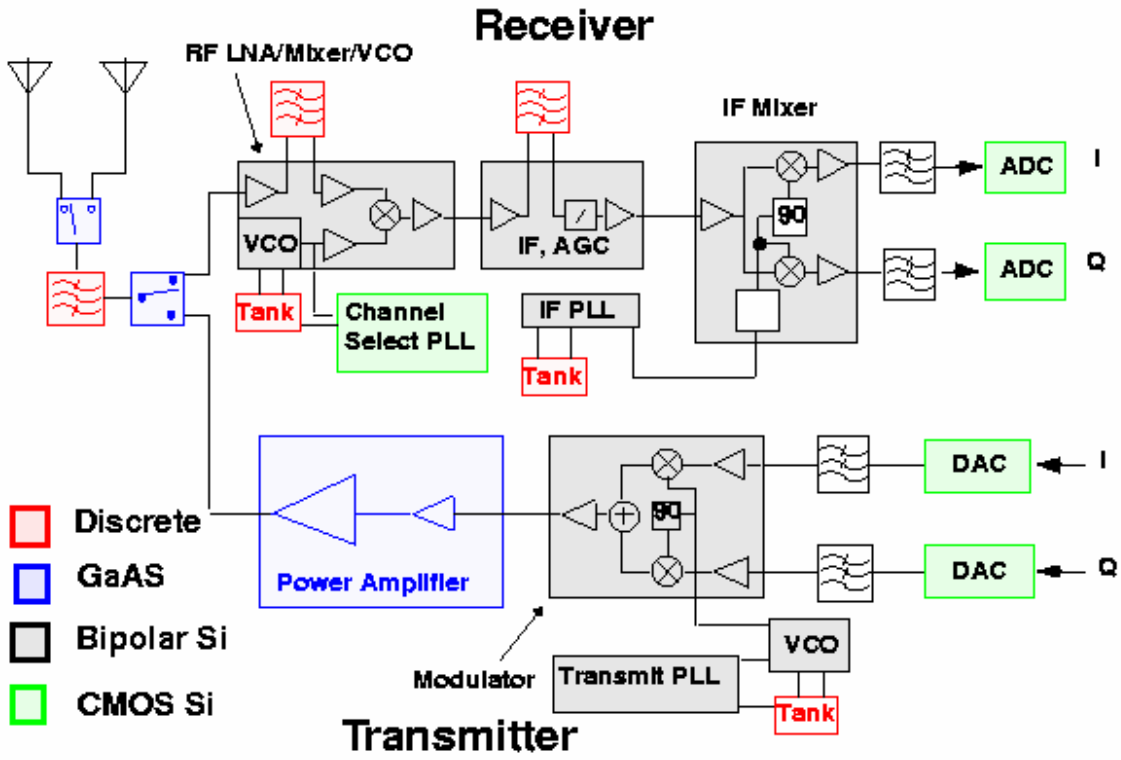


Figure 2: An illustrative picture of current transceiver [16]

Table 1: Key feature comparisons between Nokia 7210 and 8310 cell phone [41]

	Nokia 7210	**Nokia 8310**
Operating Frequency	Tri-Band EGSM 900/1800/1900	Dual band EGSM 900/1800
Weight	83 g	84 g
Size	106 x 45 x 17.5 mm	97 x 43 x 17-19 mm
Standby Time	Up to 240h	100 - 350h
Talk Time	Up to 4h	2 - 4h
Display	128 x 128 pix	84 x 48 pix
Display Color	Color display 4096 colors	Black/White
Radio	Yes (Stereo)	Yes (Mono)
Ringing Tones	Polyphonic Sounds	Monophonic Tones
GPRS	Yes	Yes
WAP Browser	WAP 1.2.1	WAP 1.2.1
Applications	$Java^{TM}$	No
Multimedia Messaging	Yes	No
Handsfree Speaker	Yes	No

with the voltage controlled oscillators (VCOs) are required to be on board. In addition, those off-chip filters, such as RF prefilter, image rejection filter, and IF filter that are now basically ceramic or surface acoustic wave (SAW) filters, need to be replaced by on-chip filters. That is why there is always a strong interest in integrating the RF filters on chip with mainstream deep-submicron CMOS technology. The main difficulties in integrating RF filters on-chip are:

1. High DR requirement. Since RF filter is the block right after/before antenna

Table 2: Demands of future-generation wireless systems [36]

Wireless System Trends	**Implications for RF/Wireless Products**
✓Higher Spectral Efficiency	✓Higher Operating Speed
✓Higher Data Rates	✓Higher Linearity
✓Capable of Handing Codes	✓Yes (Mono)
✓Multi-standard Interoperability	✓Higher Levels of Integration
✓Low Power, Smaller, and Lighter	✓Software becomes Key

in receiver/tranmitter path, the DR requirement is usually very high (>55 dB). This high DR requirement is difficult to achieve due to two reasons. First, linearization at GHz frequencies becomes very difficult because we cannot use feedback to improve the distortion. Second, the limited quality factors of on-chip passive elements available in current CMOS technologies usually require a lot of active loss compensation that inevitably increases noise. Consequently, it turns out that the DR requirement is the most important factor to enable RF filters on-chip.

2. The need for automatic tuning circuits. This is probably the second most important factor to enable RF filters on-chip. For RF filters, even they are band-selected, the required Q is still relatively high (typically, 20∼60), which makes them very sensitive to the process, voltage, and temperature (PVT) variations. High frequency operation also makes the tuning design very difficult.

3. Low-power requirement. This requirement is true especially for mobile applications. As more and more functions are integrated, the design is facing more and more battery life problems. Power management will help, but in general we would prefer low-power designs for mobile applications.

4. High CMRR and PSRR requirements. As both digital and analog parts are integrated on the same chip, differential configuration becomes a commonplace technique to prevent noise coupling which calls upon good CMRR. Good CMRR can be deteriorated by the shrinking transistor sizes as matching becomes a more serious problem. Also power supply variation is a big concern due to frequent switching activities of the digital part. Hence good PSRR is desirable.

This research focuses on RF on-chip band-pass filter (BPF) design with main target for the highest possible DR with CMOS technology. As we will explain in the

following chapters, this is achieved by some innovation and the help of looser power constraints.

1.2 RF BPF architecture

RF filters are mainly used to suppress inter-modulation products due to out-of-band interferers. Ideally, we would like to design a channel selection BPF. However because of narrow channel width and high carrier frequency, the resultant filter Q is too high to achieve or will cost too much. For example, the GSM specification has a 25 MHz band width with 200 KHz channel width. For an RF carrier frequency at around 950 MHz, the filter Q should be at least 4750 (= 950 MHz/200 KHz) for just 3 dB attenuation at channel edges. Now if we design band selection RF filters instead, we will then have a filter Q at least 38 (=950MHz/25MHz) that is more reasonable. Therefore we will design RF band selection BPF to attenuate the out-of-band interferers. For this reason, when we later calculate SFDR, we integrate the noise power spectrum density (PSD) over the total band width for noise calculation.

By putting a low noise amplifier (LNA) before the RF BPF, we can get better noise figure (NF), but receivers can be desensitized due to the strong interferers nearby. If we put the RF BPF first instead, then we will have high NF due to the insertion loss (IL) of the filter but we will have better rejection of interferers, which is more important. Therefore, we will assume that the designed RF BPF will immediately follow the antenna and is in the front of LNA.

In order to select the correct RF BPF architecture, let's first take a look at the characteristics of different types of filters shown in Table 3. It is clear that from the point of view of noise, dynamic range, and power, the Q-enhanced LC filter is the best candidate for the wireless transceiver RF filter application. Although a G_m-C filter operating in GHz range was reported recently [55], it is shown [24] that, compared with the G_m-C filter, the Q-enhanced LC filter roughly has Q_0 (inductor's

Table 3: A comparison of different filters [1]

Filter Type	**Advantage**	**Disadvantage**	**Frequency**	**Application**
Current Mode Filters	Frequency of Operation	DR at High Q, Tuning	< 150 MHz	Moderate Q IF and Baseband Filtering
Digital Filters	Precision, DR, Programmability	Power, Area, Aliasing, ADC, Clock	< 10 MHz	Low IF, Baseband Filtering and Signal Processing
Electro Acoustic Filters	DR, Stability	Process Modifications, Area	> 100 MHz	RF Preselection, IF Filtering
Gm-C Filters	Frequency of Operation	DR at High Q, Tuning	< 150 MHz	Moderate Q IF and Baseband Filtering
Passive LC Filters	DR, Stability	Q, Area	> 100 MHz	PA Harmonic Suppression, Low Q RF Preselection
Q-enhanced LC Filters	DR, Stability	Area, Tuning	> 100 MHz	RF Preselection, IF Filtering
Switched Capacitor Filters	Precision	DR at High Q, Aliasing, Clock	< 10 MHz	Low-Freq., Moderate Q IF and Baseband Filtering

Q) times less noise and Q_0 times more linearity. Hence, a total of ${Q_0}^2$ improvement in the dynamic range is seen in addition to a power saving if the same capacitor values are used. The simplified diagrams for G_m-C filter and Q-enhanced LC filter are shown in Figure 3. The theoretical derivations for DR performance of G_m-C filter [28] are illustrated by (1) – (3). Notice that in order to maximize the G_m-C filter's DR, we need to pick the transconductances $g_{m1} = g_{m2} = g_m$ and the capacitors $C_1 = C_2 = C$ [17].

$$v^2_{n,G_m-C} = \frac{KT\xi(1+2Q)}{C} \tag{1}$$

$$v^2_{o,-1dB,G_m-C} = \frac{v^2_{g_m,-1dB}}{Q} \tag{2}$$

$$DR_{G_m-C} = \frac{v^2_{o,-1dB,G_m-C}}{v^2_{n,G_m-C}} \approx \frac{1}{Q^2}\frac{v^2_{g_m,-1dB}C}{2KT\xi} \tag{3}$$

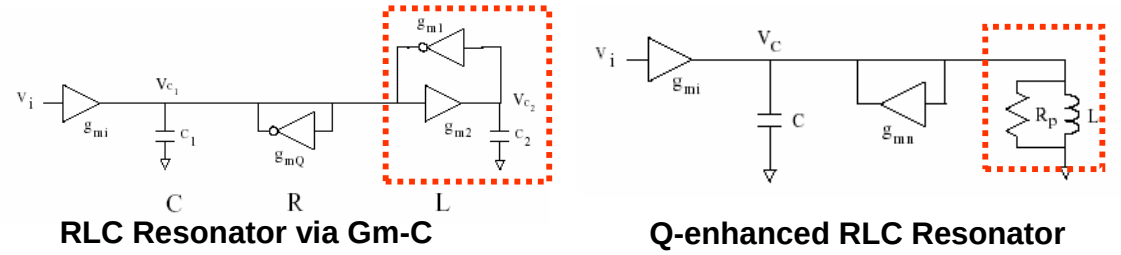


Figure 3: An illustrative picture of G_m-C filter and Q-enhanced LC filter [28]

where K is the Boltzmann constant, T is the absolute temperature in Kelvin, ξ is the excess noise factor of the transconductor which typically ranges between 1 and 2, Q is the filter Q, and

$$\omega_0 = \frac{g_m}{C}, Q = \frac{g_m}{g_{mQ}}, R = \frac{1}{g_{mQ}}$$

The theoretical derivations for DR performance of Q-enhanced LC filter [44] are illustrated by (4) – (6). Table 4 shows an experimental performance comparison of four state-of-the-art RF BPFs published recently, one G_m-C type, three Q-enhanced LC type but with different structures and negative resistance compensation schemes.

$$v_{n,Q}^2 = \frac{1}{Q_0}\frac{KT(1+\xi)Q}{C} \tag{4}$$

$$v_{0,-1dB,Q}^2 = Q_0\frac{v_{g_m,-1dB}^2}{Q} \tag{5}$$

$$DR_Q = \frac{v_{o,-1dB,Q}^2}{v_{n,Q}^2} = \frac{Q_0^2}{Q^2}\frac{v_{g_m,-1dB}^2 C}{KT(1+\xi)} \tag{6}$$

where Q_0 is the inductor Q and

$$\omega_0 = \frac{1}{\sqrt{LC}}, Q = \frac{R_P}{\omega_0 L(1-g_{mn}R_P)}, R = \frac{-1}{g_{mn}}$$

With the above theoretical and experimental results, we can conclude that:

1. In order to achieve higher DR, we need use Q-enhanced LC filter instead of G_m-C filter.

Table 4: Experimental performance comparison of four RF filters

	Wu [55]	**Li [30]**	**Chet [49]**	**Kuhn [27]**
Filter Type	2nd order $G_m - C$	4-pole Butterworth Q-enhanced	6-pole Chebyshev Q-enhanced	2-pole Q-enhanced
Technology	0.35μm CMOS	0.25μm BiCMOS	0.25μm CMOS	0.5μm SOS
Die Area	$0.2 \times 0.14\ mm^2$	$3.4 \times 2.1\ mm^2$	$1.3 \times 2.7\ mm^2$	-
Center Frequency	0.4–1.0 GHz	1.882 GHz	2.14 GHz	0.9 GHz
BW	12.5–500 MHz	150 MHz	60 MHz	20 MHz
IL	15 dB	2 dB	0 dB	11 dB Gain
Attenuation	-	-	24 dB at 1.9 GHz, 27 dB at 2.5 GHz	-
Power	17 mA	18 mA	7 mA	13 mA
VDD	3.0 V	3.0 V	2.5 V	3.0 V
$P_{1dB}/IIP3$	-/-15dBm	-9.5/0dBm	-13.4/-4.9 dBm	-5.5/0dBm
Output Noise Peak PSD	-147 dBm/Hz	-156 dBm/Hz	-155 dBm/Hz	-142 dBm/Hz
SFDR	28	49	56 [a]	56 [b]

[a] 3.84MHz BW
[b] 1MHz BW

2. There is not much DR performance difference between higher order Q-enhanced LC filters and a single LC tank. Therefore, if we don't care much about the attenuations in stop-bands, we should start with a simple Q-enhanced LC tank BPF structure for its simplicity and easy tunability.

3. Power consumption is directly related to the achievable Q of mainly the on-chip inductor. That is why in addition to higher DR, for lower power consumption, the three Q-enhanced LC filters shown in Table 4 all avoid the use of an epi-substrate. Li [30] and Chet [49] use bulk substrate and Kuhn [27] uses SOS.

4. The noise PSDs, when referred to the input side, interesting enough, are all

comparable to a 1 KΩ resistor which has a PSD of around -155 dBm/Hz at room temperature. This gives us a benchmark point when we design Q-enhanced LC filters. For example, as we will show later, based on this observation, it does not hurt our noise performance much if we simply use a 50Ω resistor for input matching.

1.3 Research contributions

Based on what we have concluded in Section 1.2, this thesis focuses on a single Q-enhanced LC tank BPF design to achieve better DR performance. Specifically, it uses a divide-and-conquer method by designing:

1. A new simple pseudo-differential pair (PDP) for input g_m stage. It is the fastest high-linearity, low-distortion, wide-range, and constant–g_m design reported to date. This has been applied in the final filter tape-out and proven experimentally.

2. A new tunable discrete inductor (TDL) to achieve two-level inductance with the same real estate that can be used to expand the filtering frequency range. This has been verified experimentally.

3. A new tunable discrete capacitor (TDC) to achieve high linearity over wide terminal voltage swing range. This has been verified through simulation.

4. The design of a Q-enhanced LC filter in a new systematic way to achieve synchronized gain, center frequency, and filter Q tuning capability. This has been verified through simulation.

The fabricated 900 MHz filter, with NSC's standard 0.18 μm digital epi–substrate CMOS technology, achieves the highest DR so far even with an inductor Q of just around 1 compared with a typical value > 8 in the previous published work.

1.4 Thesis organization

The thesis is organized as follows. In Chapter 2, the new ideas to linearize the input operational transconductance amplifier (OTA) are illustrated. Since the filtering function is mainly accomplished by the LC tank, we will talk about the on-chip capacitor and inductor design in Chapter 3. The new systematic way to achieve synchronized gain, center frequency, and filter Q tuning capability is explained in Chapter 4 with two supporting simulated BPFs. The tape-out filter is shown in Chapter 5 with the measurement results. Chapter 6 concludes this thesis with future work.

CHAPTER 2

OTA LINEARIZATION TECHNIQUES [31]

The transconductance cell (g_m-cell) is one of the most universal building blocks finding wide applications in the design of amplifiers, LNAs, and filters. It is generally required to have:

1. High linearity to allow large signal swings, which is the upper limit of dynamic range.

2. Low noise for good lower limit of dynamic range.

3. No dominant internal poles for high-speed operation capability.

4. Low-power for portable applications.

Among all the above requirements, linearity is probably the most challenging requirement as the I-V relation of MOS transistor is inherently nonlinear.

In this chapter, we will first review the previous linearization techniques in Section 2.1. One new simple way to extend the linearization range by superposing several shifted copies of existing OTA is presented in Section 2.2. By identifying that at GHz frequencies only a current differencing method is effective in linearizing the OTA, a very simple wide-range, low-distortion, and constant-g_m building block called PDP suitable for high-speed applications is presented in Section 2.3. For a 0.18 μm CMOS typical process, 1.8 V supply, simulation results show that over 1.1 VPP differential input range, gm variations can be maintained within $\pm$0.15%. At 100 MHz, the total harmonic distortion (THD) is less than -64 dB; and at 10 GHz, THD $<$ -39 dB. It is the fastest, wide-range, and low-distortion constant-g_m reported to date considering

that the best performance so far is -61 dB THD up to 20 MHz over 3.6 VPP with 3.3 V supply voltage [9], which was reported in 2002.

2.1 Previous linearization techniques

Linearization techniques found in the literature can be broadly classified [14] as:

1. Adaptive biasing.
2. Class-AB operation.
3. Source degeneration.
4. Triode constant g_m.
5. Current differencing.

They are explained in more details in the following sections.

2.1.1 Adaptive biasing technique

The adaptive biasing technique [52] is illustrated in Figure 4. The idea is to generate a biasing current of

$$I_{SS} = I_{SS,DC} + kV_{id}^2 \tag{7}$$

Assume

$$I_D = \frac{\beta}{2}(V_{GS} - V_T)^2 \tag{8}$$

then

$$I_o = I_{D1} - I_{D2} = \begin{cases} \sqrt{\beta I_{SS,DC}} V_{id} \sqrt{1 - \frac{(\beta - 4k)V_{id}^2}{4I_{SS,DC}}} & \mid V_{id} \mid \leq \sqrt{\frac{2I_{SS}}{\beta - 2k}} \\ I_{SS,DC} + kV_{id}^2 & \mid V_{id} \mid \geq \sqrt{\frac{2I_{SS}}{\beta - 2k}} \end{cases} \tag{9}$$

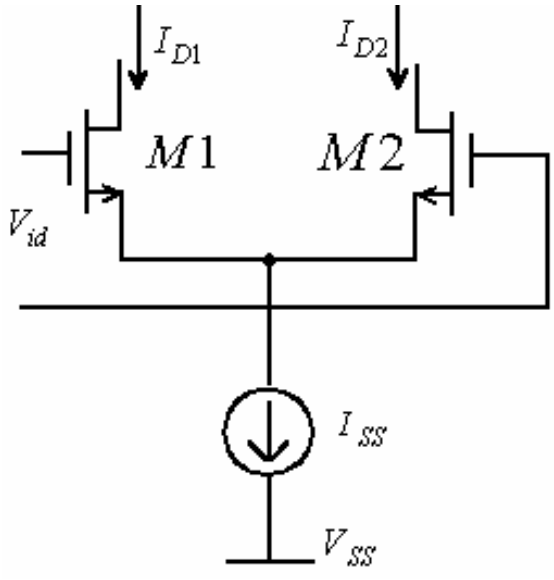


Figure 4: Simple differential pair g_m

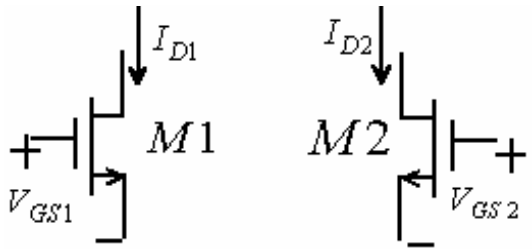


Figure 5: Two transistors used for class-AB g_m

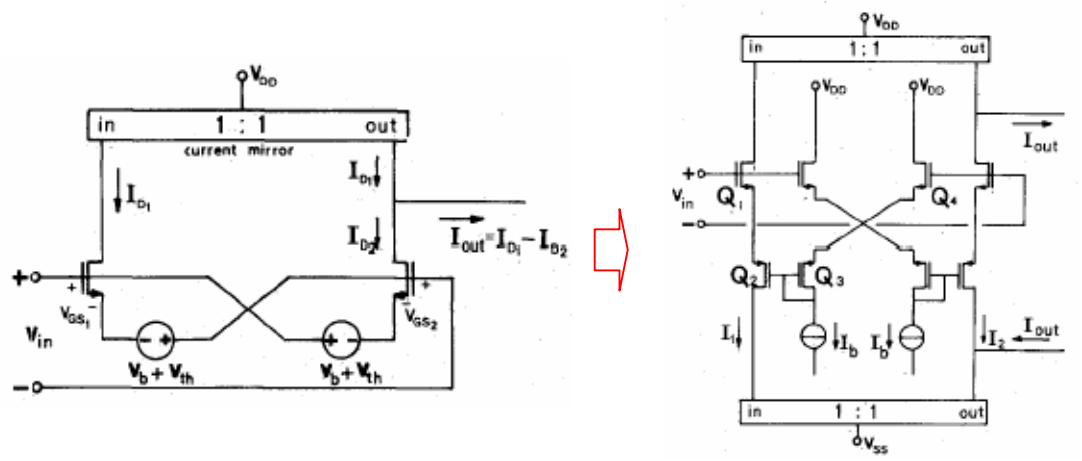


Figure 6: One example of class-AB g_m implementation

2.1.2 Class-AB operation technique

The class-AB operation technique is shown in Figure 5. The key idea is to keep the sum of V_{GS1} and V_{GS2} constant.

Assume

$$I_D = \frac{\beta}{2}(V_{GS} - V_T)^2 \tag{10}$$

then

$$I_o = I_{D1} - I_{D2} = \frac{\beta}{2}(V_{GS1} + V_{GS2} - 2V_T)V_{id} \tag{11}$$

One example of class-AB g_m is illustrated in Figure 6 [48]. Another example of class-AB g_m is illustrated in Figure 7 [12].

2.1.3 Source degeneration technique

The key idea of source degeneration is illustrated in Figure 8. The source degeneration provides a feedback mechanism converting the inherently nonlinear transconductance of the transistor itself to an equivalent constant g_m that is referred to a constant source degenerated resistor (which, for example, can be a poly resistor with good voltage and temperature stability). A couple of implementation examples [54] are shown in Figure 9.

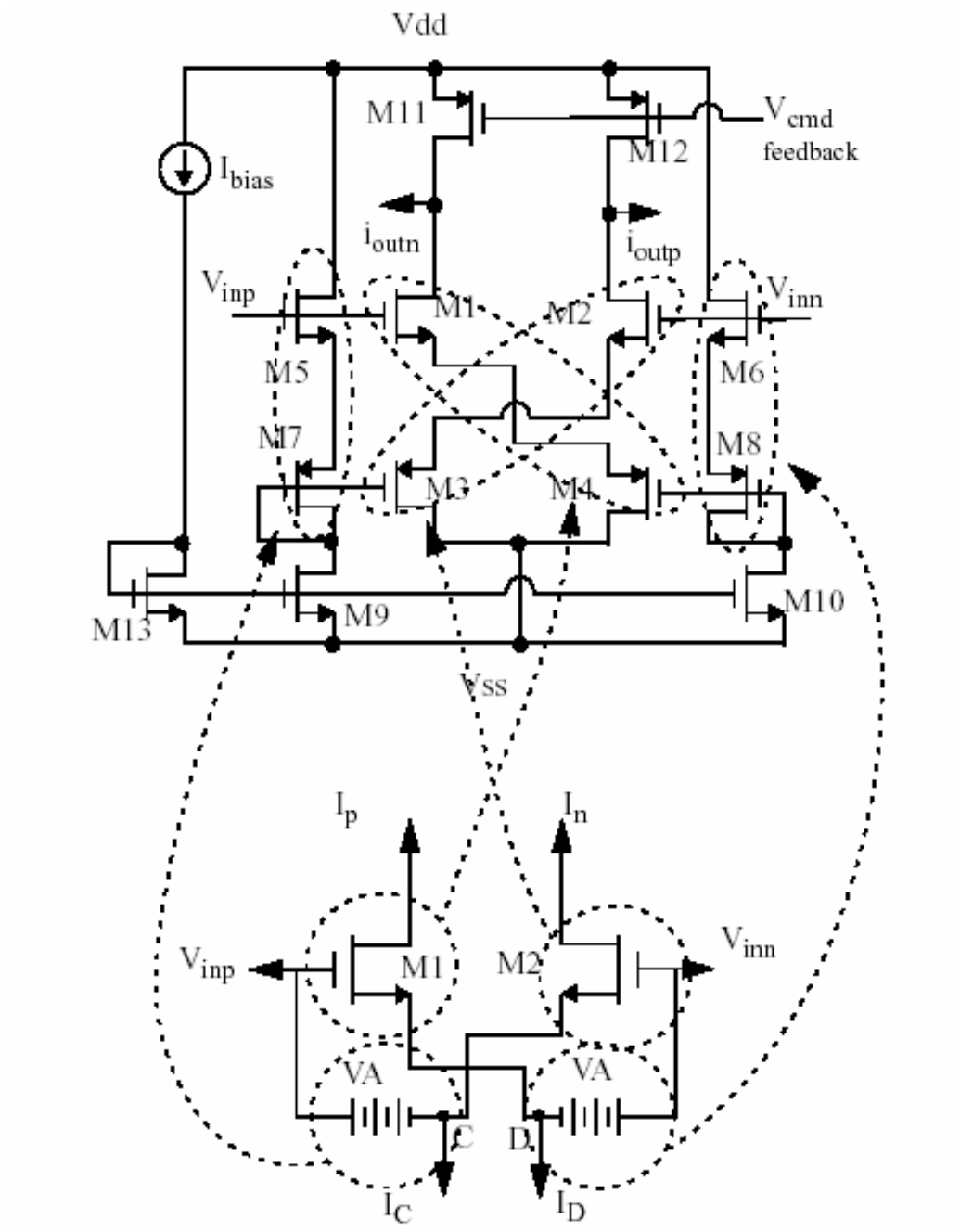


Figure 7: Another example of class-AB g_m implementation

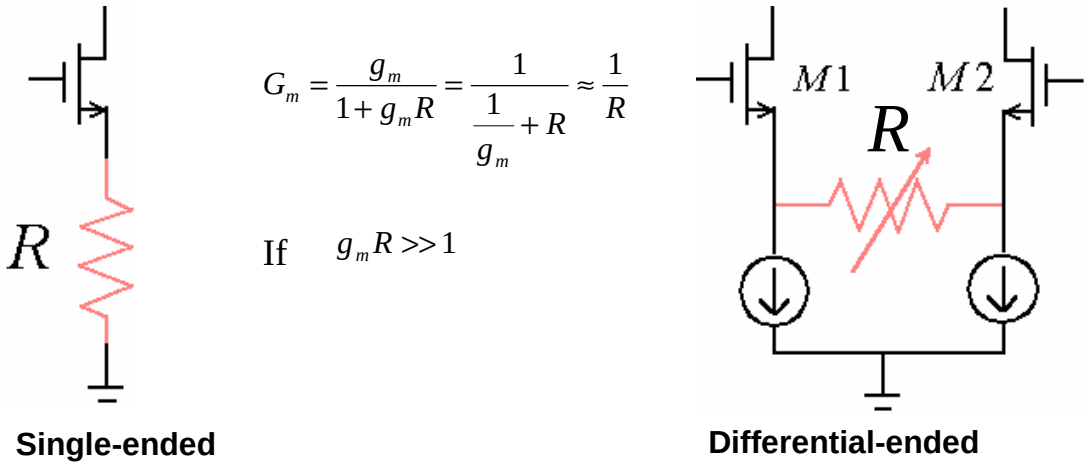


Figure 8: Source degeneration for constant g_m

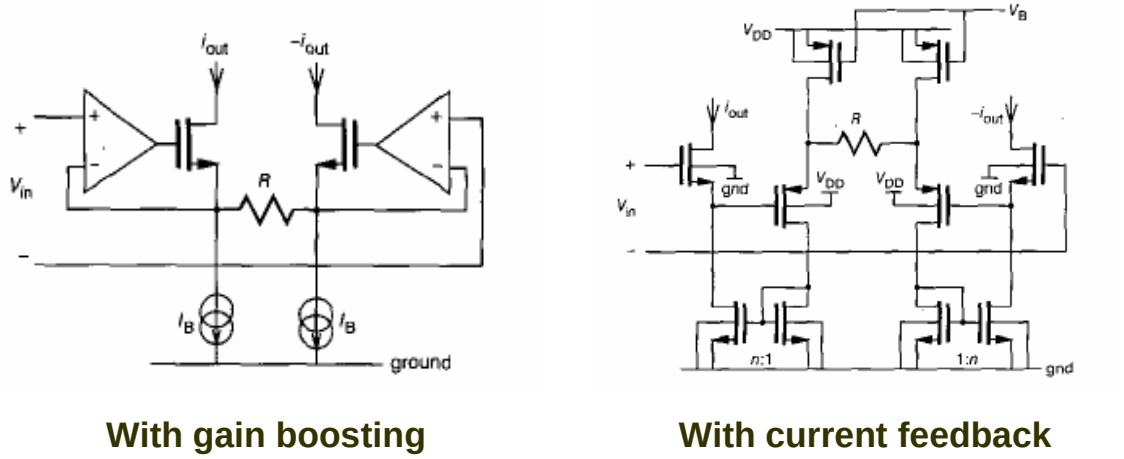


Figure 9: Source degeneration constant g_m examples.

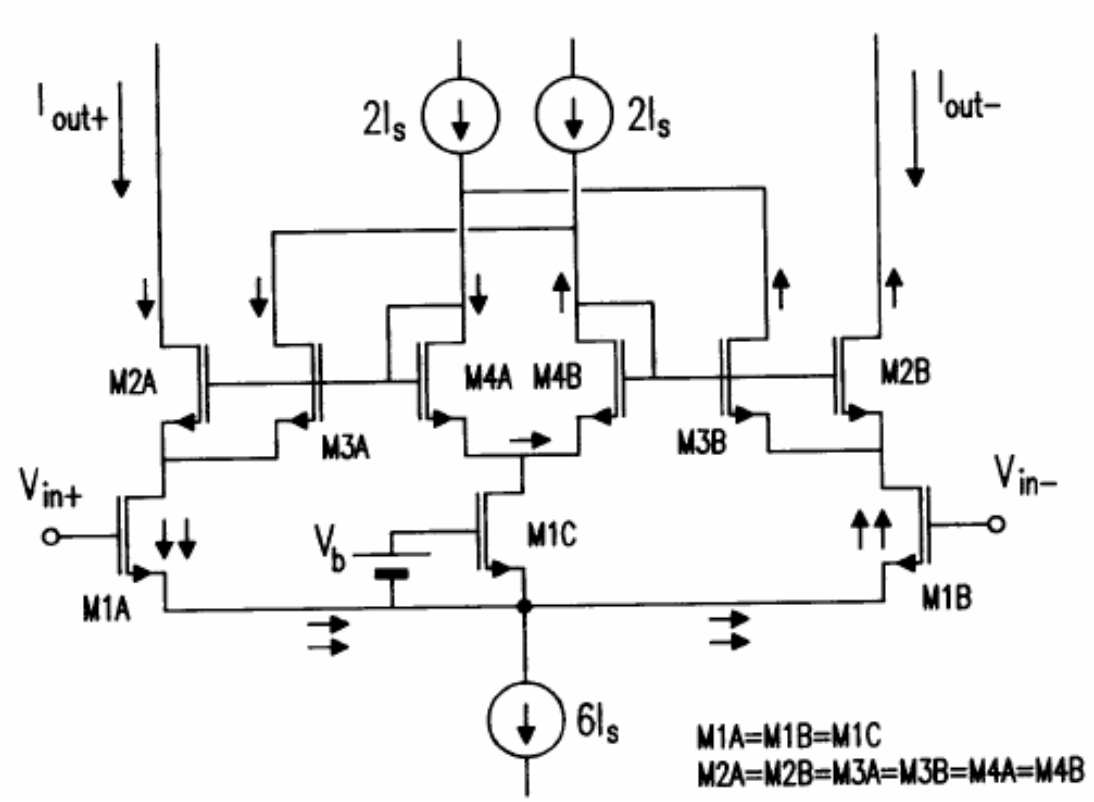


Figure 10: Triode constant g_m example.

2.1.4 Triode constant g_m technique

This is based on the observation that when MOS transistor is biased in deep triode region [46], i.e. if $V_{DS} \ll 2(V_{GS} - V_T)$, then

$$I_D \approx \mu C_{OX} \frac{W}{L}(V_{GS} - V_T)V_{DS} \tag{12}$$

It is therefore crucial to keep the V_{DS} constant for a constant g_m. One example of triode g_m circuit implementation [38] is illustrated in Figure 10.

2.1.5 Current differencing technique

The idea of the current differencing technique [53] [20] is to obtain a linear I-V relation by canceling the nonlinear terms with current differencing. The best linearity is obtained by the well-known four-transistor transconductor circuit (but with more

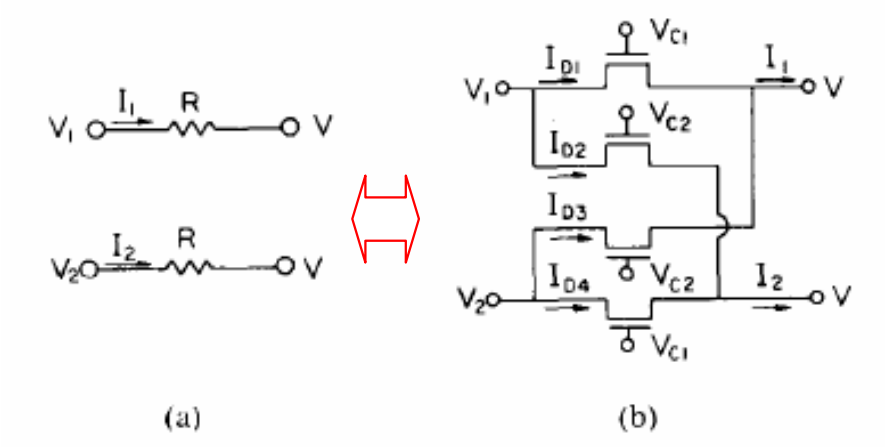


Figure 11: The double-MOSFET method for nonlinearity cancellation (a) resistor pair R (b) equivalent MOS structure

noise) found wide applications in MOSFET-C filter. This is illustrated in Figure 11 [20].

Assuming all the transistors stay in triode, i.e.,

$$V_1, V_2 \leq min[V_{C1} - V_T, V_{C2} - V_T] \tag{13}$$

then

$$I_O = I_1 - I_2 = \frac{1}{R}(V_1 - V_1) \tag{14}$$

where

$$\frac{1}{R} = \frac{1}{R_1} - \frac{1}{R_2} = \mu C_{OX} \frac{W}{L}(V_{C1} - V_{C2}) \tag{15}$$

Among the above five linearization techniques, the first four usually involve some form of feedback mechanism or stacking of many transistors. Hence they suffer from either a limit speed or a limit large signal swing. The best performance reported to date is -61 dB THD up to 20 MHz [9]. The current differencing method has been successfully used to generate linear R in MOSFET-C filter applications [20]. Without using any feedback, it appears to be the only candidate for high-speed OTA design. However the above current differencing method usually biases the transistors in triode region hence with a limited voltage swing. In Section 2.3, a new g_m-cell inspired by

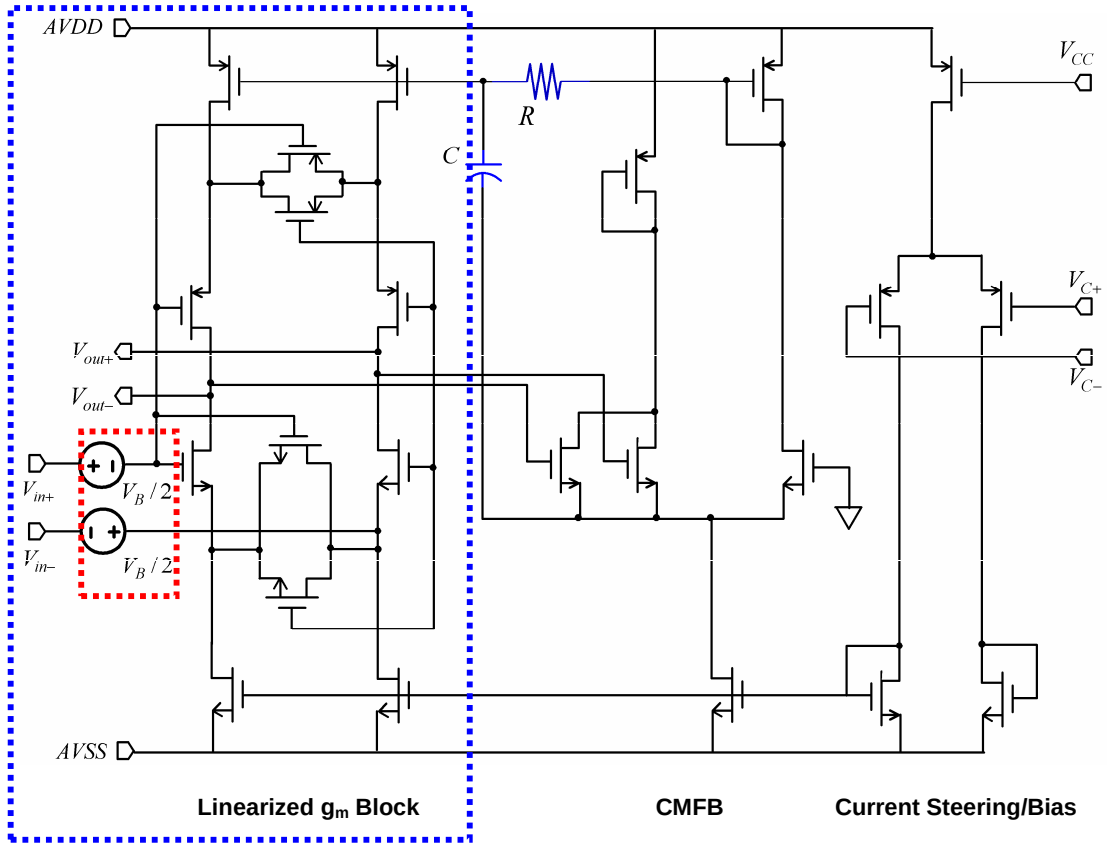


Figure 12: One copy of linearized g_m block (CMOS version)

the EKV model shown in Figure 14 [56] has been designed using current differencing with all transistors biased in saturation. Before we introduce that, let's first look at a new way to extend the linearization range with existent linearization techniques such as the most popular source degeneration technique in Section 2.2.

2.2 A new linear range extension technique by superposition

With the existent linearization techniques such as the most popular source degeneration technique [25], we can use batteries to shift the center operating points and superpose them to extend the available linear range of constant-g_m. One example circuit is illustrated in Figure 12. The simulation results are shown in Figure 13.

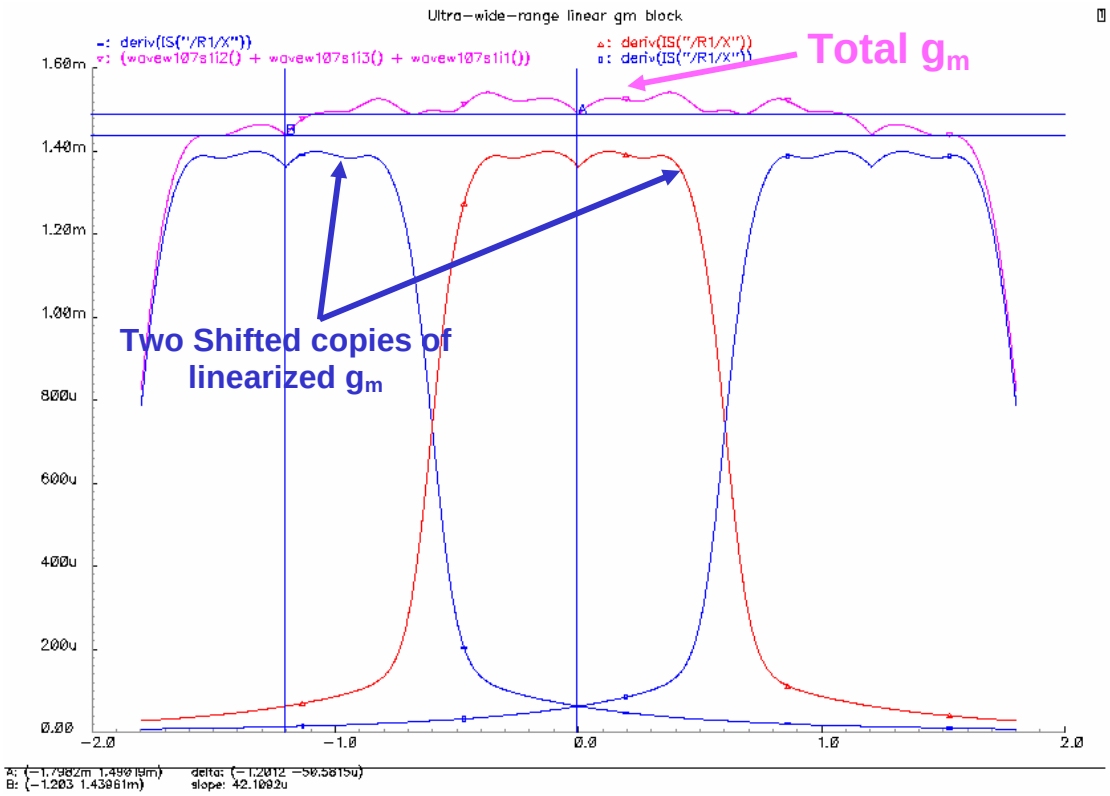


Figure 13: Simulation results to demonstrate the new linear range expansion technique by superposing three shifted copies of the g_m block shown in Figure 12. Now over nearly full voltage swing from -1.7∼+1.7 V (1.8 V supply voltage), $-3.4\% < \frac{\Delta g_m}{g_m} < 3.5\%$.

The main difficulty in implementing this idea is to design very good voltage buffers and shift these g_m copies by a proper amount. None of these tasks are trivial. In addition, it is obvious that this solution is to trade the linear range with power and noise performances. In order to solve these problems, more innovations are needed. It turns out that we can do much better without losing much power and noise performance with the new PDP circuit that we will cover in Section 2.3.

2.3 Another new linearization technique by current differencing

The explanation of MOSFET operating in triode region with EKV model is briefly summarized in Section 2.3.1 followed by the new g_m-cell design presented in Section 2.3.2. Theoretical derivation using alpha-power law MOSFET model is presented in Section 2.3.3 to explain the linearization mechanism of PDP. Simulation results are given in Section 2.3.4.

2.3.1 Single MOS transconductor

The most simple constant-g_m block is a single-MOS transconductor operating in triode region with constant drain-source voltage as shown in Figure 14 [56]. Using the EKV MOS transistor model [15], the drain current I_D of a strong inversion NMOS transistor can be represented by the difference between square-law forward current I_F and reverse current I_R as shown in (16) with I_F and I_R given in (17) and (18) respectively.

$$I_D = I_F - I_R \tag{16}$$

$$I_F = \begin{cases} \frac{n\beta}{2}(V_P - V_S)^2 & V_S < V_P \\ 0 & V_S > V_P \end{cases} \tag{17}$$

$$I_R = \begin{cases} \frac{n\beta}{2}(V_P - V_D)^2 & V_D < V_P \\ 0 & V_D > V_P \end{cases} \tag{18}$$

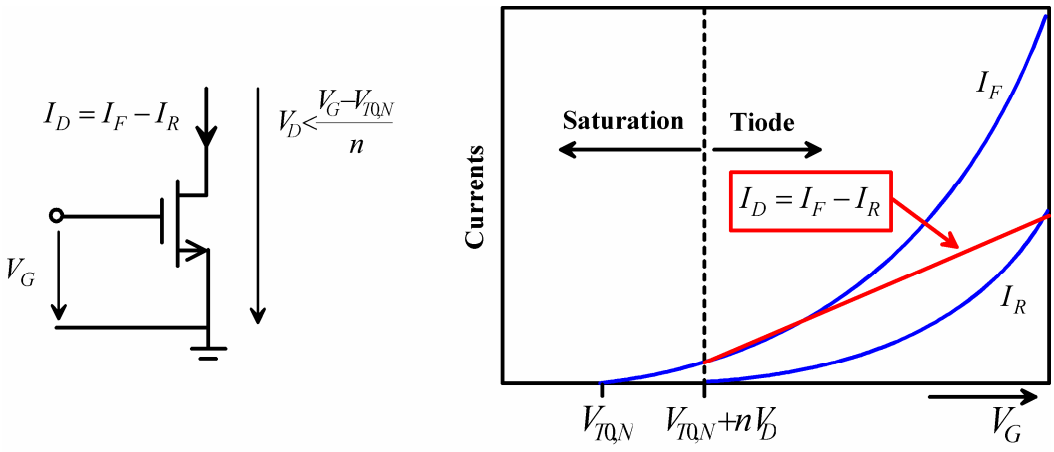


Figure 14: Single-MOS transconductor operating in triode region

where n is the slope factor, $\beta = \mu C_{OX}\frac{W}{L}$, $V_P = \frac{V_G - V_{T0,n}}{n}$ is the pinch-off voltage, $V_{T0,n}$ is the threshold voltage, and V_G, V_D, and V_S is the gate, drain, and source voltages referred to the substrate respectively. Notice that if $V_G < V_{T0,n}+nV_D$, then the NMOS transistor will operate in saturation region with only the I_F part, the conventional Shockley square law model. Otherwise it will operate in triode region with both I_F and I_R resulting a g_m of βV_D which is directly proportional to the variation of V_D indicating unity sensitivity between them, which is very undesirable. To get around this problem while using the same mechanism to obtain constant-g_m, the following PDP circuit is proposed.

2.3.2 PDP circuit

The proposed new PDP cell is shown in Figure 15. The inductors L are kept there for a possible RF filter application configuration. A differential structure is used for common-mode rejection and even harmonic suppression. All transistors have the same sizes. With V_B near supply voltage VDD, input biased at the middle-supply VDD/2, all transistors stay in strong inversion and saturated, and have almost equal and close to maximum overdrive voltages. Transistors MF1 and MF2 provide the

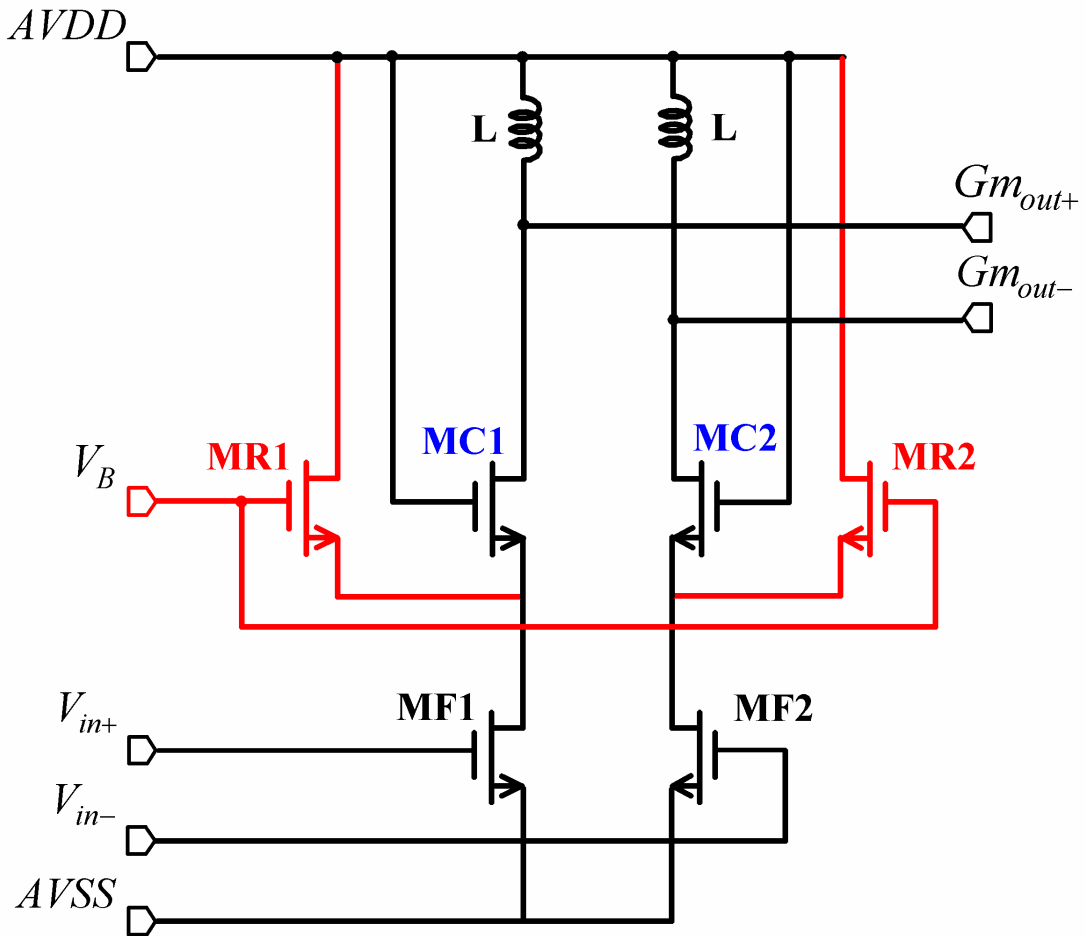


Figure 15: Proposed pseudo-differential pair constant-g_m cell

forward current part in (16) that subtracts the reverse current part in (16) from MR1 and MR2. The resulting difference currents are taken from MC1 and MC2. MC1 and MC2 also act like cascode transistors to isolate the input and output and reduce the Miller effect for higher speed operation.

2.3.3 Theoretical derivation of PDP circuit

In the late 80's, Sakurai and Newton found out that due to velocity saturation, Shockley square law model failed to predict MOSFET's drain saturation voltage and drain current in the saturation region as the channel length shrunk down to submicron

values. They invented an alpha-power law MOSFET model and successfully predicted a more accurate CMOS inverter delay [47]. Almost 9 years later, Bowman et al. further extended this idea and came up with a physical-based alpha-power law MOSFET model to include the sub-V_T region operation, both vertical and lateral mobility degradation and velocity saturation, and threshold voltage roll-off [4]. However Bowman's model is not very suitable for hand-calculations as it has around 20 parameters. In addition, lots of the parameters are related to the process and are usually confidential. Therefore, we will restrict our explanation in a general sense without going too many details. We will explain how the technology scaling helps to obtain constant-g_m and how the PDP achieves a cancelation of the 3rd order output current harmonics resulting in a constant-g_m by proper biasing. We will explain the tradeoff between the power and linearity and how to design the PDP in general. The Bowman's physical alpha-power law MOSFET model in the saturation region (the region that we are interested in) is described in (19). Details can be found in Figure 2 of [4].

$$I_{DSAT} = I_{D0}(\frac{V_{GS} - V_T}{V_{DD} - V_T})^{\alpha} \tag{19}$$

$$I_{D0} = \frac{W}{L} \frac{\mu_0 C_{OX} V_{D0}[V_{DD} - V_T - (\eta/2)V_{D0}]}{[1 + \theta(V_{GS} - V_T)][1 + V_{DSAT}/(E_C L)]} \tag{20}$$

$$\alpha = \frac{1}{\ln(2)} \ln\left(\frac{2V_{D0}[V_{DD} - V_T - (\eta/2)V_{D0}]}{V_{Da}[V_{DD} - V_T - \eta V_{Da}]}\right) \tag{21}$$

One feature of Bowman's model is that the dependence of carrier velocity on V_{GS} is jointly described by I_{D0} and α. When the product of critical electrical field and channel length $E_C L$ becomes larger than the overdrive voltage $V_{GS} - V_T$, the MOSFET will experience less and less carrier velocity saturation resulting larger I_{D0} and α. With $E_C L \gg V_{GS} - V_T$, the MOSFET is considered to operate in long-channel region and α tends to 2 and the Shockley square law applies. If $E_C L \ll V_{GS} - V_T$, the MOSFET will experience severe carrier velocity saturation and drain current in

saturation region will approach a linear dependence of the overdrive voltage $V_{GS} - V_T$ or α will tend to 1 which indicates a constant g_m. As a matter of fact, to the first order approximation [4] [29],

$$g_m = \frac{\mu_0 C_{OX}}{2} E_C W \tag{22}$$

which is linearly scalable with channel width W.

Intuitively, as α changes from 2 to 1 with the scaling down of technology, the I-V relation is more linear resulting more constant g_m. More rigorously, by examining the following binomial expansion:

$$\begin{aligned}(X + \Delta x)^\alpha = X^\alpha + \alpha X^{(\alpha-1)}\Delta x + \frac{\alpha(\alpha-1)}{2!} X^{(\alpha-2)}\Delta x^2 \; |\Delta x| \leq X \\ + \frac{\alpha(\alpha-1)(\alpha-2)}{3!} X^{(\alpha-3)}\Delta x^3 + \ldots \quad 1 \leq \alpha \leq 2\end{aligned} \tag{23}$$

where X represents the DC biasing part, Δx the signal swing part and the convergence region $|\Delta x| \leq X$ physically corresponds to the saturation requirements, two observations from (23) can be made as α tends to 1 from 2:

1. The higher order terms get smaller, which means a more linear I-V relation, a desirable feature.

2. The linear term gets smaller resulting a smaller available g_m, a undesirable feature.

Now let's apply Bowman's formula and (23) to see how the 3rd order current harmonics gets canceled in the PDP. For the simplicity of analysis, all transistors have the same sizes. We will focus on the left leg of the differential structure, i.e., MC1, MR1, and MF1 part. First, notice that due to body effect, threshold voltages of MR1 and MC1 are bigger than that of MF1, which means MF1 will experience more velocity saturation, i.e. I_{D0MF1} and α_{MF1} will be smaller. The exact values can be calculated using Bowman's physical formula with the process data and assuming a

biasing (a good starting point is that assuming that V_B is also tied to VDD. The actual value will be a little smaller.). Second, notice that V_S, the source voltage of MR1 and MC1, is about VDD/2, 0.9 V. The change, ΔV_S, will be approximately linear with the input voltage swing, ΔV_{IN} with a coefficient of around -0.7 for long-channel, -0.5 for short-channel. For first-cut estimation, we can assume $\Delta V_S = -0.6\Delta V_{IN}$. Then we have,

$$I_{DMC1} = I_{DMF1} - I_{MR1} \tag{24}$$

$$I_{DMF1} = I'_{D0MF1}(V_{IN} - V_{TMF1} + \Delta V_{IN})^{\alpha_{MF1}} \tag{25}$$

$$I_{DMR1} = I'_{D0MR1}(V_B - V_S - V_{TMR1} + 0.6\Delta V_{IN})^{\alpha_{MR1}} \tag{26}$$

Notice that I'_{D0MF1} and I'_{D0MR1} have included the constant terms $(1/(V_{DD} - V_{TMF1})^{\alpha_{MF1}})$ and $(1/(V_{DD} - V_{TMR1})^{\alpha_{MR1}})$ for simplicity. Using (23), in order to cancel the 3rd order harmonics, we need a unique V_B that can be solved through (27):

$$I'_{D0MF1}\begin{pmatrix}\alpha_{MF1}\\ 3\end{pmatrix}(V_{IN} - V_{TMF1})^{(\alpha_{MF1}-3)} = I'_{D0MR1}\begin{pmatrix}\alpha_{MR1}\\ 3\end{pmatrix}(V_B - V_S - V_{TMR1})^{(\alpha_{MR1}-3)} \tag{27}$$

With this V_B, the g_m can be calculated through (28):

$$\begin{aligned} g_m = {} & I'_{D0MF1}\alpha_{MF1}(V_{IN} - V_{TMF1})^{(\alpha_{MF1}-1)} \\ & - I'_{D0MR1}\alpha_{MR1}(V_B - V_S - V_{TMR1})^{(\alpha_{MR1}-1)}(0.6) \end{aligned} \tag{28}$$

Notice the subtraction clearly shows a tradeoff between power and linearity. Using the above equations, with all transistors sized at 27 μm/0.3 μm, V_B is calculated to be 1.52 V and g_m of 5.7 mS. These values are in good agreement with actual simulation results of 1.61 V and 4.7 mS. The discrepancy mainly comes from the fact that actual MR1 suffers less short-channel effect than MC1 due to $V_B < VDD$. Accurate results

can be obtained via iterations. One key feature of PDP is that its power and available g_m are all linearly scalable with the channel width W. Hence it is only necessary to design V_B once via a DC sweep, then scale the sizes to obtain the desired g_m. Another tradeoff of this PDP design is poor CMRR/PSRR v.s. high linearity as there are no head and tail current sources. Also constant-g_m biasing circuitry is a must for the PDP.

2.3.4 Simulation results of PDP circuit

The PDP cell has been simulated with NSC's 0.18 μm standard digital CMOS process using Cadence spectreS simulation tool. With VDD = 1.8 V, the inputs are biased at 0.9 V. Instead of comparing performances with [9] at frequencies up to 20 MHz (the upper capability limit of [9] with THD < -61 dB) as the results are already exceptionally good, the PDP is intended to operate at GHz range while having comparable performances. With the same power constraints, all transistors are sized at 27 μm/0.3 μm resulting a g_m of 4.696 mS. Minimum channel length 0.18μm is avoided for better matching while keeping the high speed. Considering that conventional cascode g_m-cells are commonly used for RF applications such as LNA designs, it is worthwhile to compare the performances of the PDP and the cascode g_m-cells with the same g_m values. Notice that the PDP becomes conventional cascode if V_B is biased at low supply. Through a DC sweep, V_B is determined to be 1.61 V as shown in the 1st plot of Figure 16. Notice that the g_m variation is -0.3% over 1.1 VPP differential input for the PDP while -14.7% for the cascode. From the 2nd plot of Figure 16, the mechanism of generating constant-g_m through subtraction of two alpha-power-law current is quite obvious. On the same plot, cascode current is also plotted to show their curvature differences. AC simulation shown in the 3rd plot of Figure 16 indicates that both the PDP and the cascode can operate up to 10 GHz with only 10% g_m drop. THD results for 1.1 VPP differential input at 0.1, 1, and 10

Table 5: Comparison of various constant-g_m techniques and PDP

Ref.	Tech.	VDD	Power	Input	Sig. Freq.	THD
[9]	0.35 μm	3.3 V	10.56 mW	3.6 VPP	20 MHz	-61 dB
This work	0.18 μm	1.8 V	10.77 mW	1.1 VPP	100 MHz	-64 dB
					1 GHz	-48 dB
					10 GHz	-39 dB
Cascode	0.18 μm	1.8 V	6.27 mW	1.1 VPP	100 MHz	-38 dB
					1 GHz	-37 dB
					10 GHz	-36 dB

Table 6: PDP performances under process variation

	Slow	Typical	Fast
THD with 1.1 VPP at 0.1/1/10 GHz	< -58/45/39 dB	<-64/48/39 dB	< - 53/49/39 dB
g_m Variation with 1.1 VPP DC Sweep	$\pm$0.4% of 4.184 mS	$\pm$0.15% of 4.689 mS	$\pm$1.02% of 5.125 mS
g_m drop at 10 GHz via AC Simulation	15.63%	10.75%	7.66%

GHz are shown in the 4th plot of Figure 16. They are obtained through a 100-cycle transient analysis to make sure all transients die out. Notice that the cascode THD is not very sensitive to the frequencies while the PDP apparently excels below 10 GHz with up to 26 dB more THD at 100 MHz. The main performances are tabulated in Table 5. The PDP performances under process variation are tabulated in Table 6. These simulation results indicate that the PDP's performances are not very sensitive to process variations.

2.4 Summary

In this chapter, we have first reviewed the previous OTA linearization techniques and identified that at GHz frequencies only a current differencing method is effective

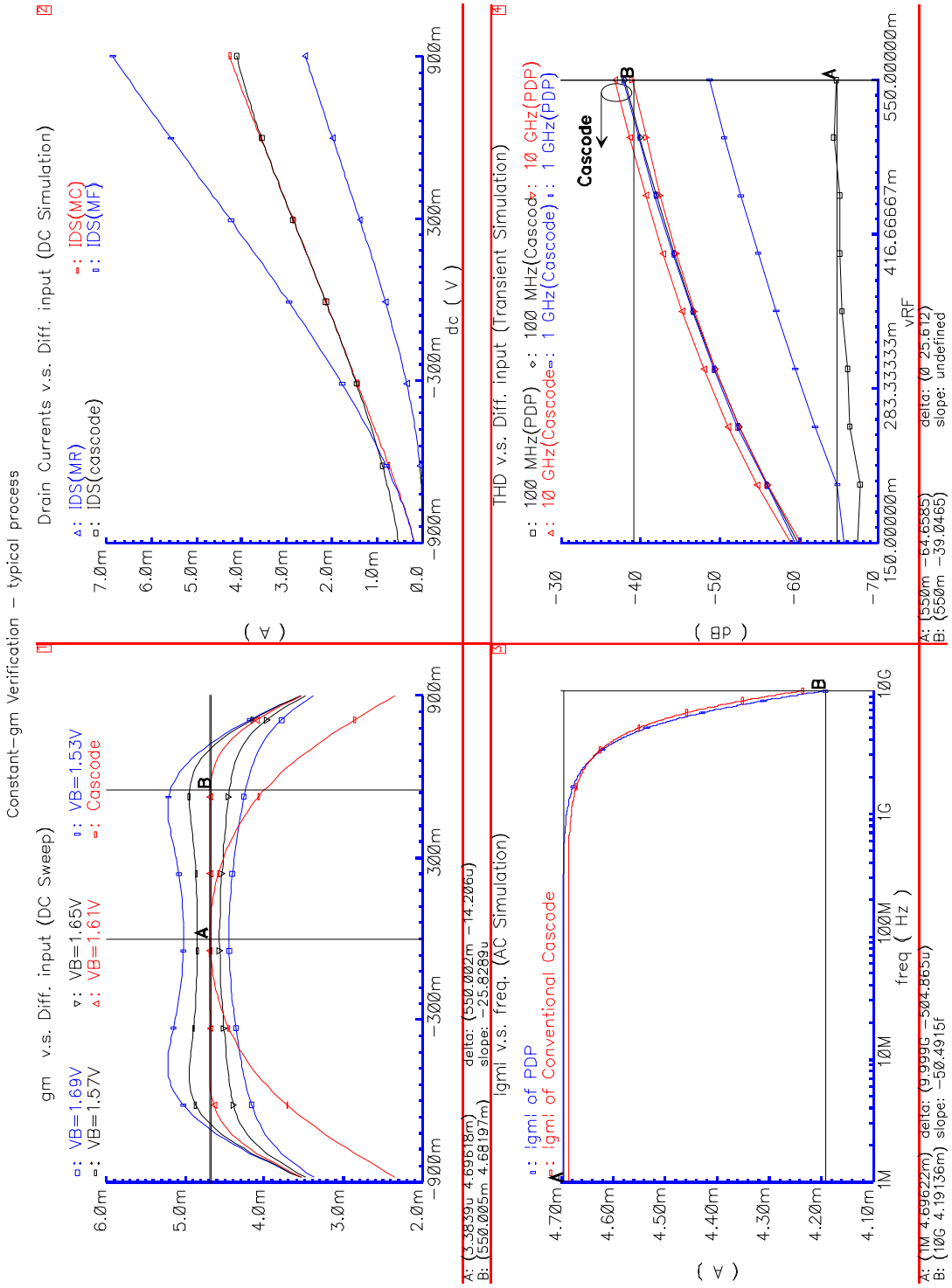


Figure 16: DC sweep (plot 1), DC simulation (plot 2), AC simulation (plot 3), and THD transient simulation (plot 4) results of PDP and conventional cascode g_m cell with the same g_m values

in linearizing the OTA. Based on the current differencing idea, we have presented a very simple wide-range, low-distortion, and constant-g_m building block called PDP suitable for high-speed applications. The simulation results verify this new design.

CHAPTER 3

LC TANK

3.1 On-chip inductors

3.1.1 Introduction to on-chip inductors

Since the introduction of the Si spiral inductor and its successful applications in LC filters operating in gigahertz range in 1990 [39], significant research has been done to better model and understand the loss mechanism, and thus enhance the Q of on-chip inductor. Among available CAD tools for inductor design, Analysis and Simulation of Inductors and Transformer for Integrated Circuits (ASITIC) [40] turns out to be one of the more up-to-data, accurate, and convenient tools to help the designer to obtain the layout and relevant electrical parameters for a particular value of inductance with a given technology. It generates the following widely accepted lumped pi-model at the given frequency as shown in Figure 17, which can serve as an analytical model for the first-cut design. It is worth emphasizing that all these parameters are frequency dependent. Hence, this compact model is best suitable for narrow band applications [40].

The various loss mechanisms associated with inductors on Si are illustrated in Figure 18.

Common practices/important results to get a better quality of inductor are summarized below and they are all related to the reduction of some losses shown in Figure 18.

1. To reduce series resistance, circle- or octagon-shaped instead of square-shaped inductors [7] can be used. Line spacing should be kept to the minimum allowed by technology for more effective series loss reduction than by widening the

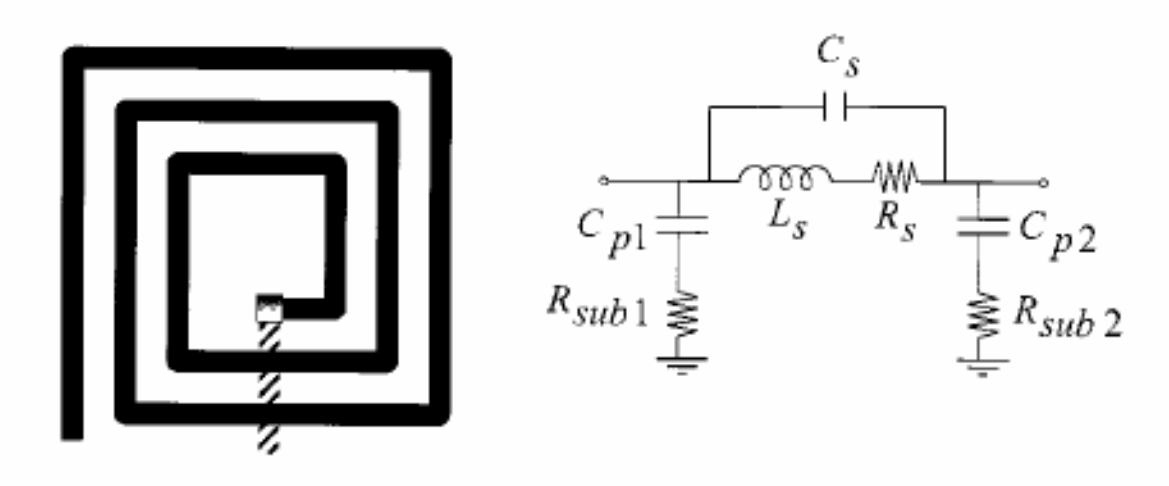


Figure 17: Top view of an on-chip spiral inductor and its physical model [49].

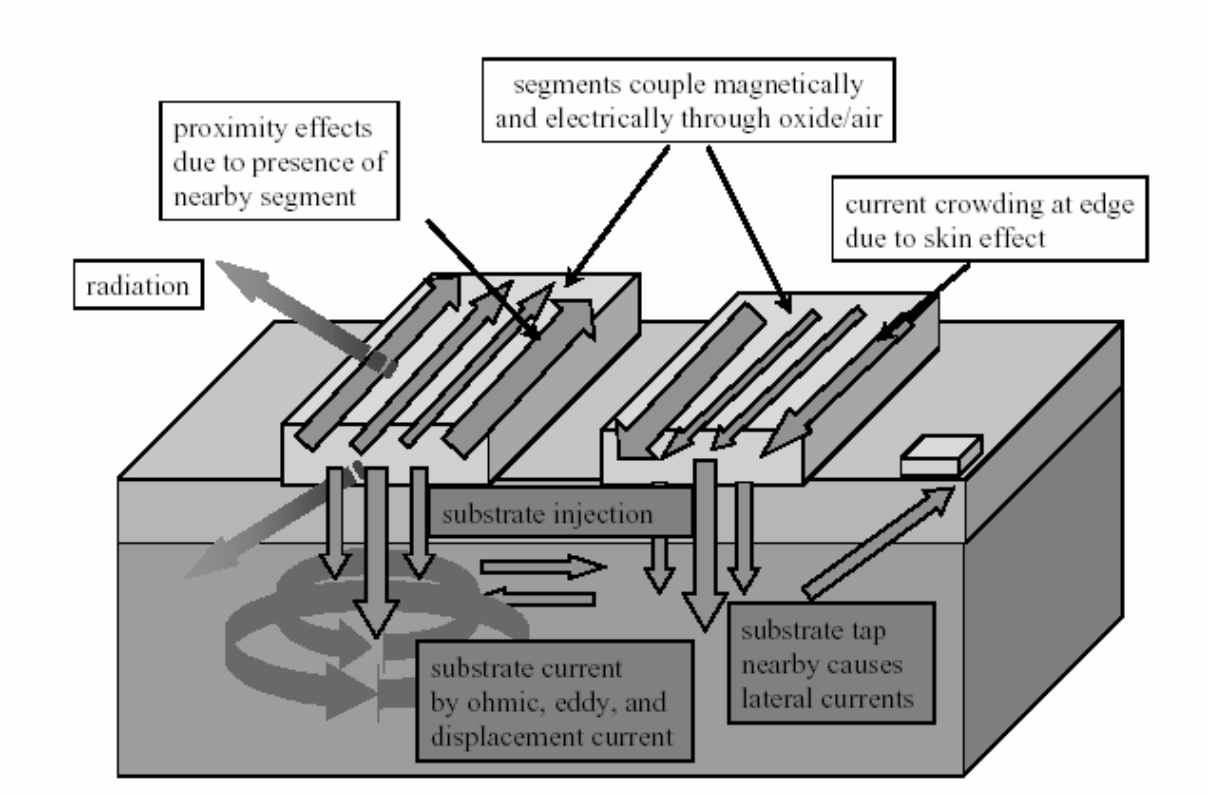


Figure 18: Various loss mechanisms presented in an IC process [40].

line [7] [57]. Low-resistivity metals such as copper can be used. To reduce the magnetically induced part of the series resistance, tapered structures [33] and hollow coils [10] can be used.

2. A patterned ground shield (PGS) [57] can be used to reduce the substrate electrical coupling between two adjacent inductors. It turns out [51] that center ground shield (CGS) works better in terms of improving the inductor's Q. One example of such layout is shown in Figure 19.

3. For differential circuit applications, symmetric structures [26] [11] can be used for better Q, higher self-resonate frequency (SRF), and less area. One example for such configuration is shown in Figure 20.

4. To get symmetric leg parameters in the pi-model of Figure 17, a symmetric structure for a single inductor can be used [40].

5. The metals can be put furthest away from the substrate to reduce the substrate coupling capacitance. Suspended inductors [8] [21] or surface micromachined solenoid inductors [23] can be used to eliminate the substrate loss and electrical coupling. A stacked structure can be used to reduce the substrate coupling capacitance and increase SRF and available inductance for the same area [35] [58].

6. Multilevel-spiral (MLS) inductors either in series or a parallel connection can be used to enhance the Q [6] [40]. To reduce the cost, it is preferable to use inductors without any post-process technologies. One example of shunting metal 5 and 4 for type B connection in Figure 20 is shown in Figure 21.

The above common practices provide us the design guidelines to get a high Q inductor. In order to make the LC tank tunable, i.e., make it resonate at different frequencies, we need to change either the capacitance or the inductance. It is common

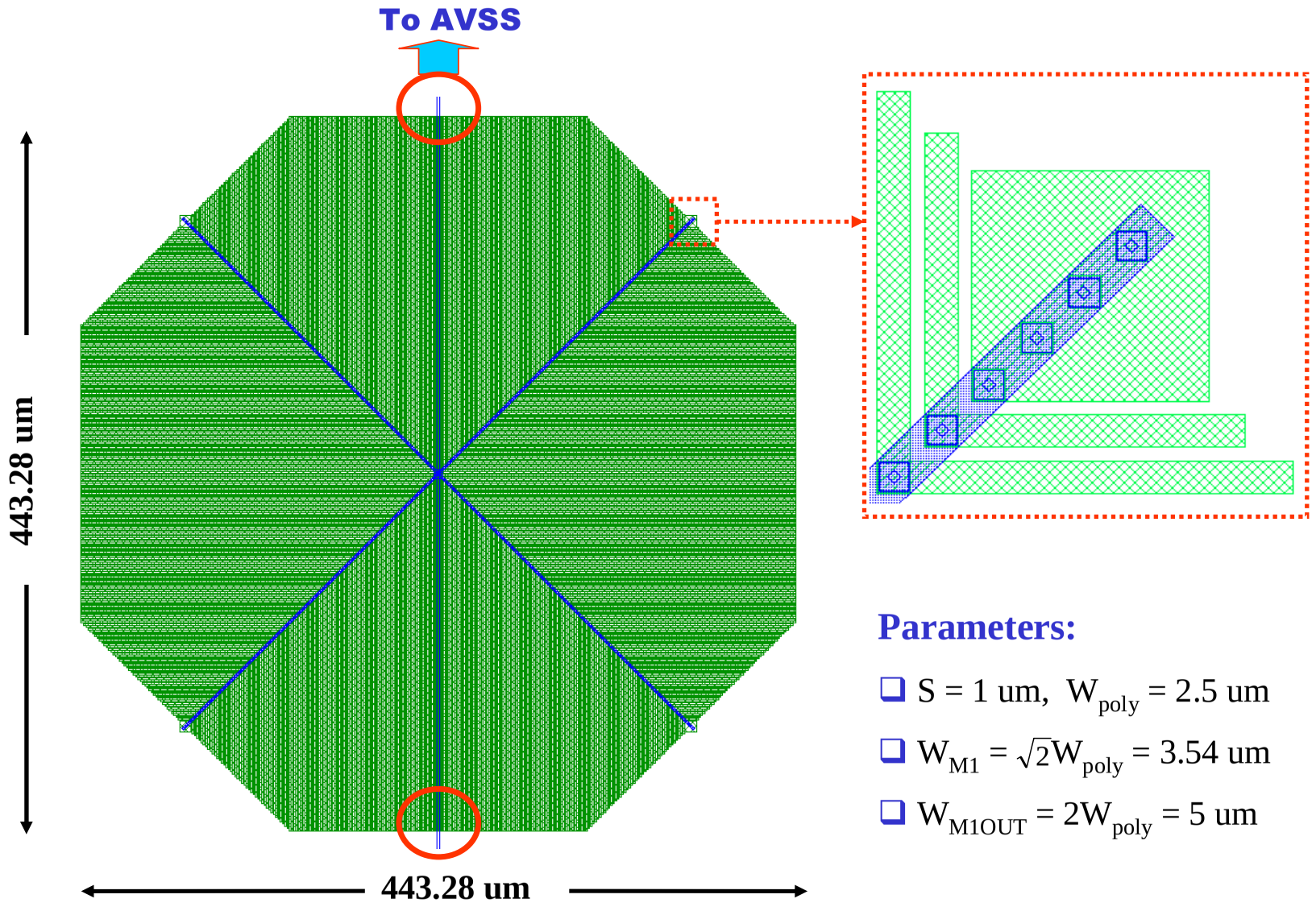


Figure 19: Layout of CGS for octagonal shape inductor.

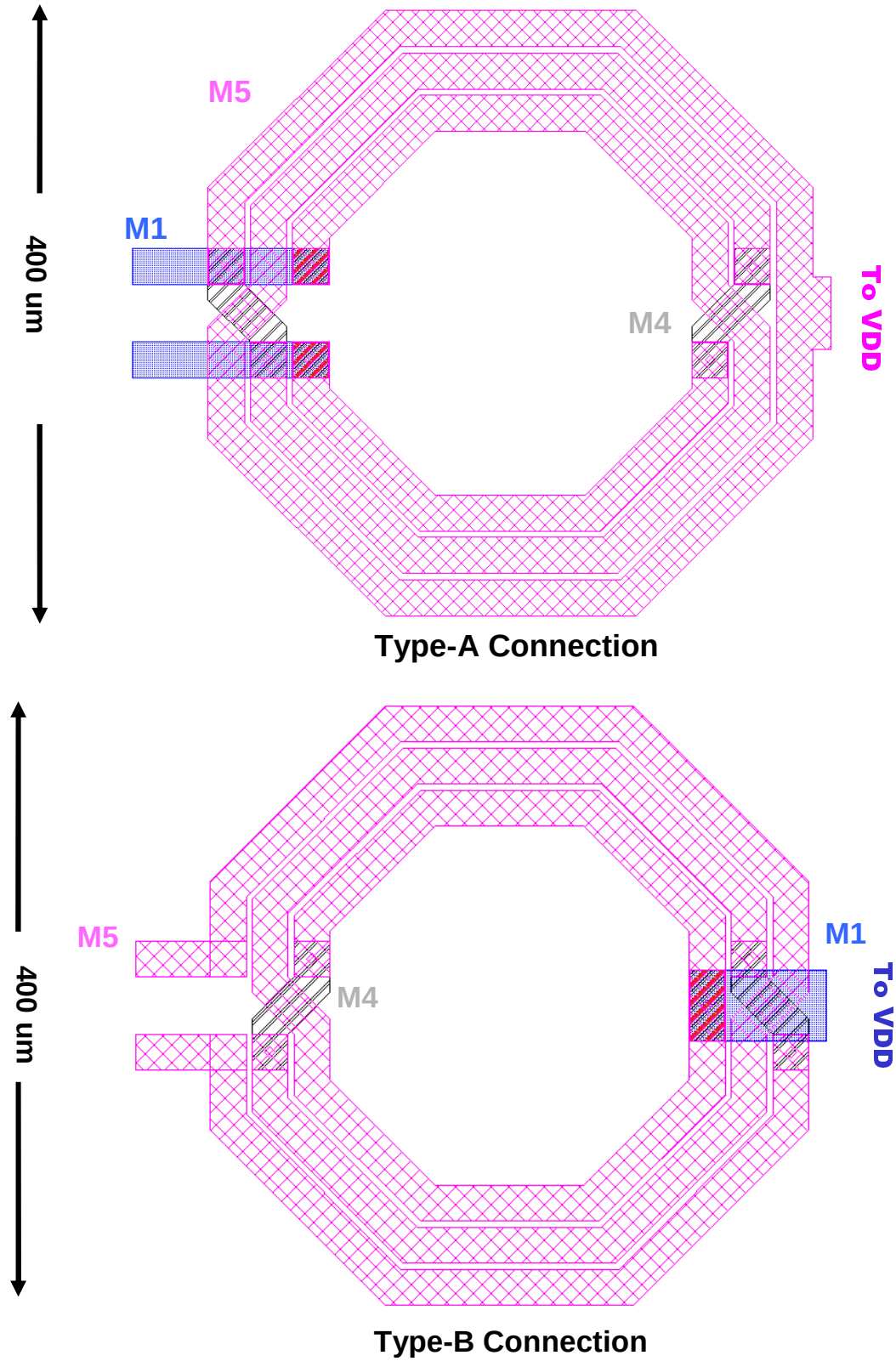


Figure 20: Layout of octagonal shape and symmetric structure inductor with two ways of connections.

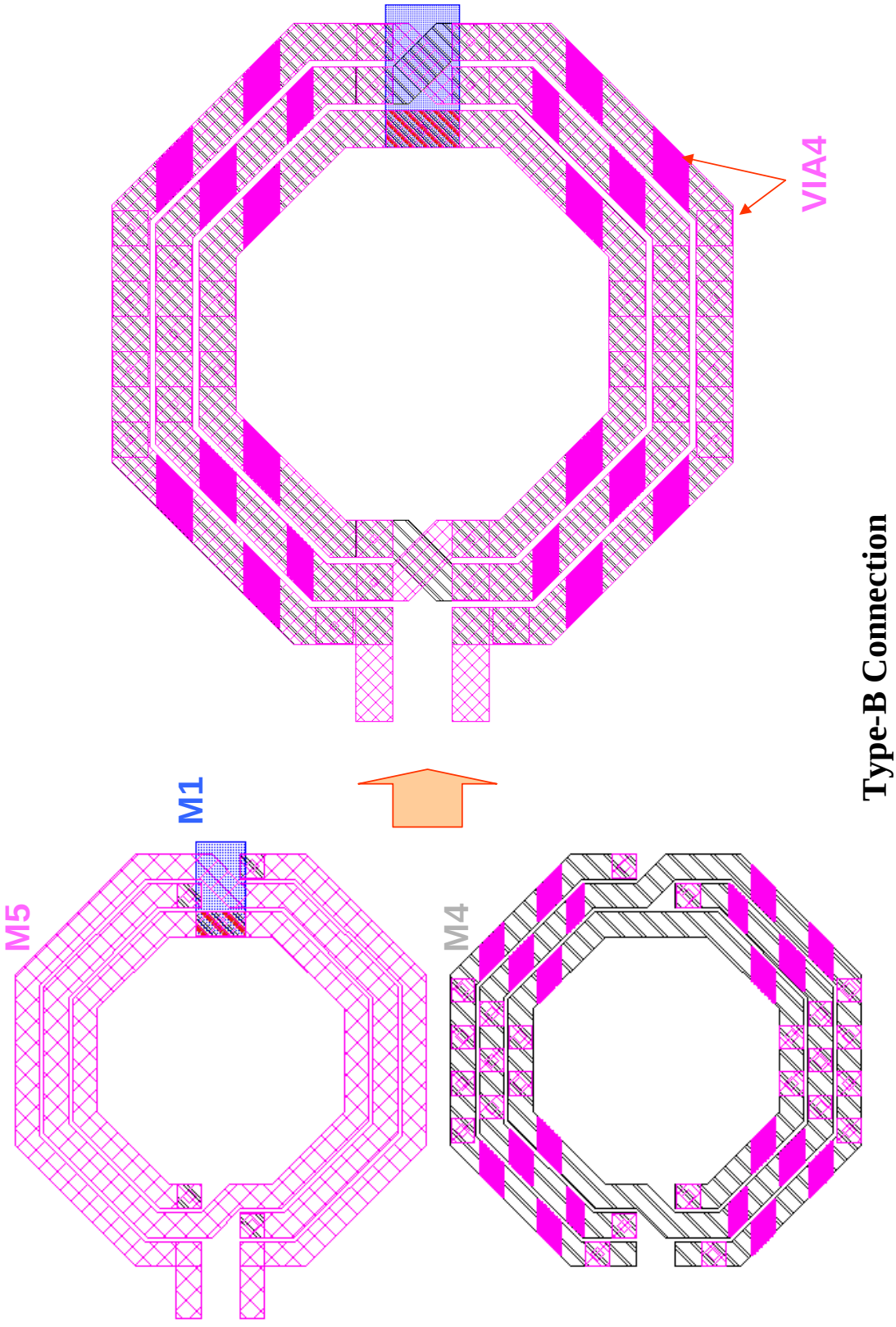


Figure 21: Inductor formed by shunting Metal 5 and 4 for type B connection in Figure 20.

to use variable capacitance as it is much easier to control the electrical field than magnetic field on-chip. However, it would be very desirable to make the inductance also tunable especially for a very wide frequency tuning capability. For example, suppose that we want to design (very ambitiously) a universal RF BPF to cover all cell phone and wireless date communication frequencies from GSM to HiperLAN shown in Figure 22, then for 1 nH fixed inductance, the capacitance needs to be tuned from ∼0.76 pF t0 ∼34.4 pF to cover the center frequency ranging from ∼858 MHz to ∼5.77 GHz. Now, suppose that we do not care much about linearity, quality etc and only care about the capacitance density, so we can use the gate capacitance. For a 0.18 μm CMOS technology, the gate capacitance density is usually on the order of 8 fF/μm^2. Therefore, a 34.4 pF capacitor will take about 4300 μm^2! To save silicon area and expand the LC tank's frequency tunability, the tunable discrete inductance design is presented in the next section.

3.1.2 A New Tunable Discrete Inductor (TDL) Design

The tunable discrete inductance design is based on the following simple transformer idea shown in Figure 23. The equivalent inductance is taken from the primary side and the secondary side is switchable. As we can see from the simplified model of transformer, when the switch is open, we get L_1 inductance, i.e., the secondary side has no effect. When the switch is closed, by Lenz's law, the secondary side will generate a counteracting magnetic field to that of the primary side, resulting an equivalent inductance of about $L1 - M$ if $L_2 \approx M$.

The layout for the TDL test structure is shown in Figure 24 with the switch part zoomed in and shown in Figure 25. The primary side is identical to the inductor that we have designed in the previous section. It uses metal 5. The secondary side is simply one turn of metal 2 with a switch implemented by a MOS transistor. The requirements for the switch are:

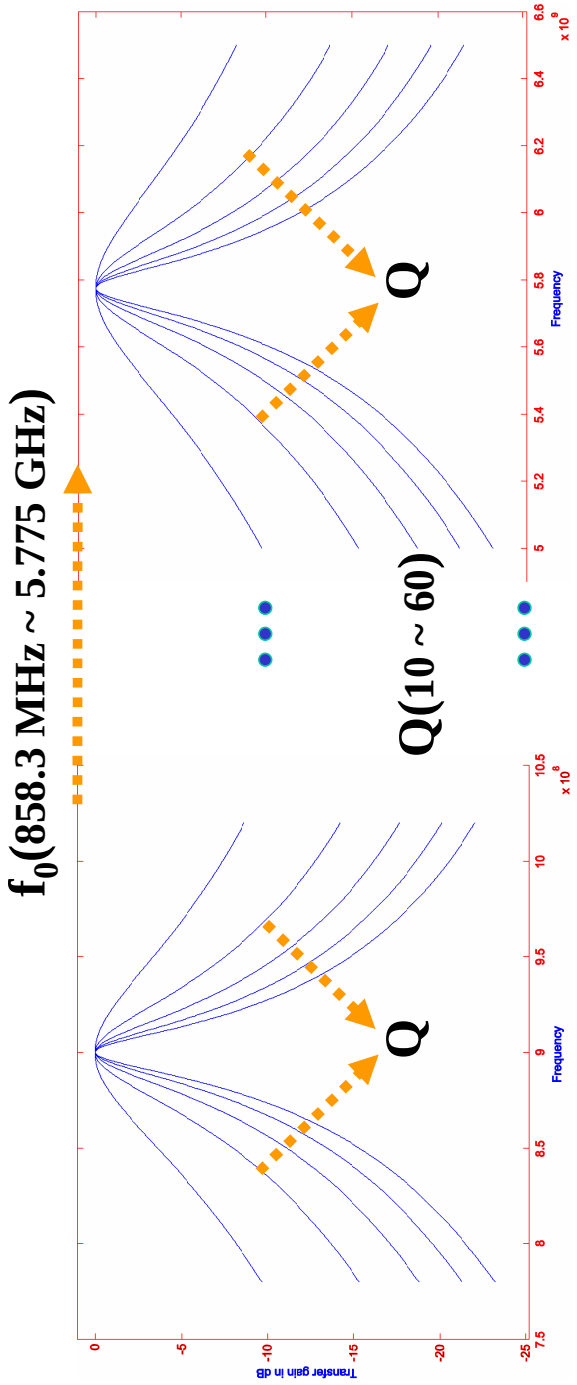


Figure 22: A universal RF BPF to cover all cell-phone and wireless date communication frequencies from GSM to HiperLAN. The filter Q is made tunable also for different DR requirements.

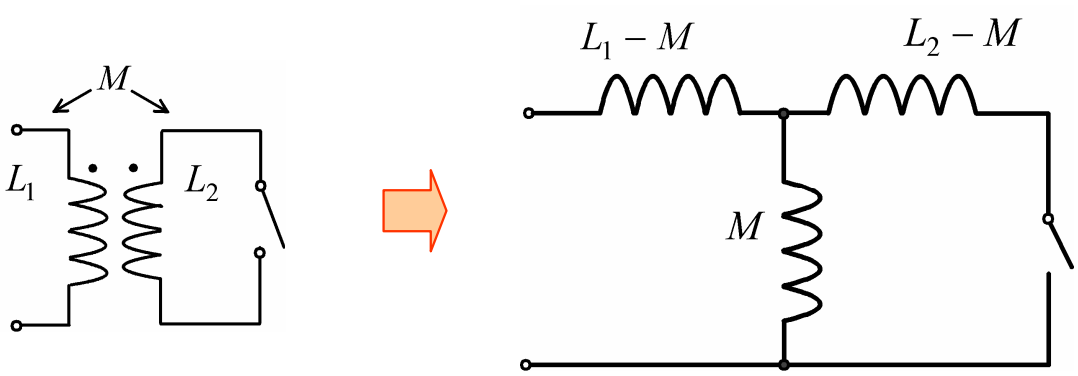


Figure 23: Transformer idea for the tunable discrete inductor design.

1. Small resistance for less loss and stronger counteracting magnetic field. This can be done by increasing the switch's W/L ratio by using the smallest channel length and multi-finger structure. In the layout example shown in Figure 25, the W/L is about 3600, resulting a resistance less than 1 Ω.

2. High-linearity for linear mutual inductive coupling. This can be achieved by putting the switch in the neutral point of secondary side as shown in Figure 24.

3. Non-floating secondary side to enable the switch to operate properly. This can be done by connecting the other neutral point opposite to the switch with the ground.

The fabricated TDL die microphotograph is shown in Figure 26. It is measured by a on-wafer probing setup. The equipment used are listed below:

1. Cascade probe station – summit 9000

2. ACP50/150 GSG-150probes

3. RF cables upto 50GHz

4. WinCal 3.1 with LRRM calibration standard

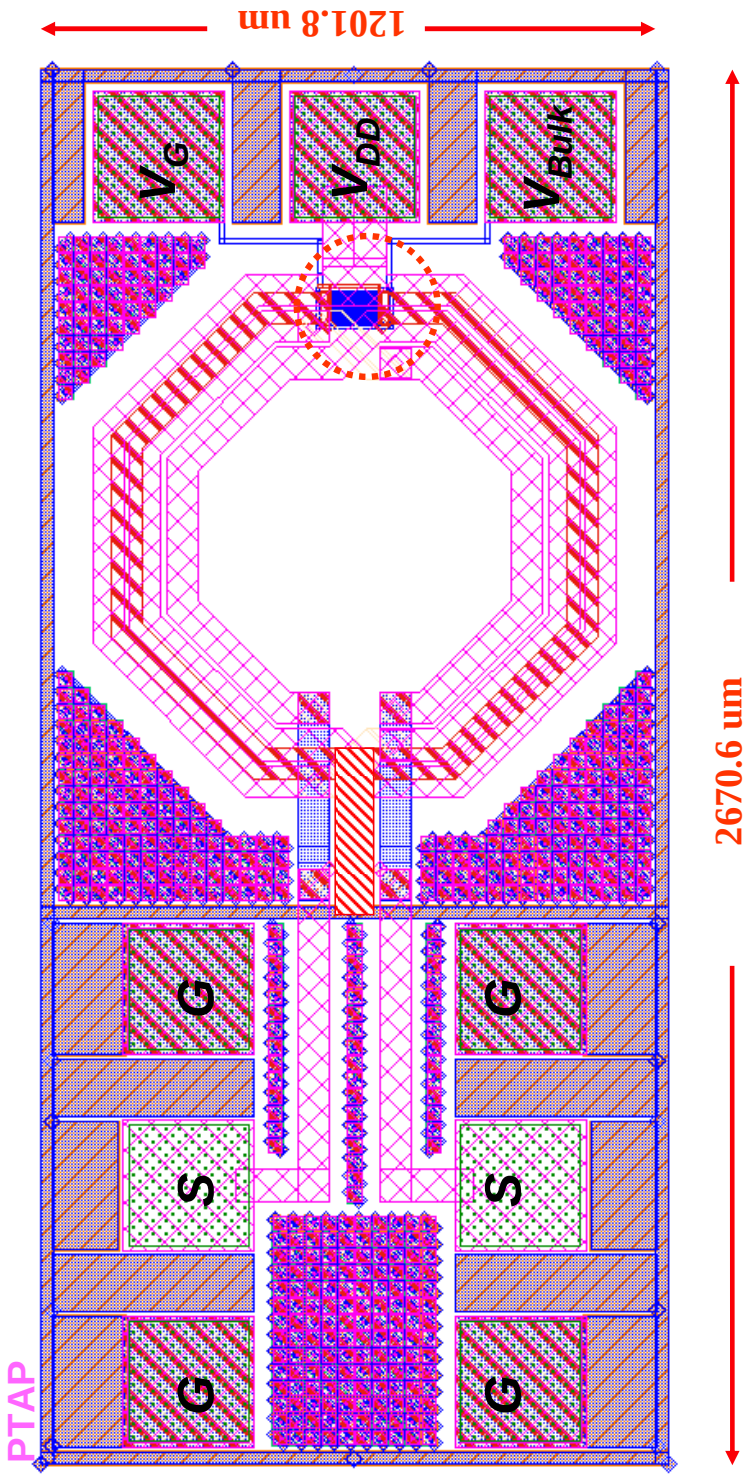


Figure 24: Testing structure layout for the tunable discrete inductor design.

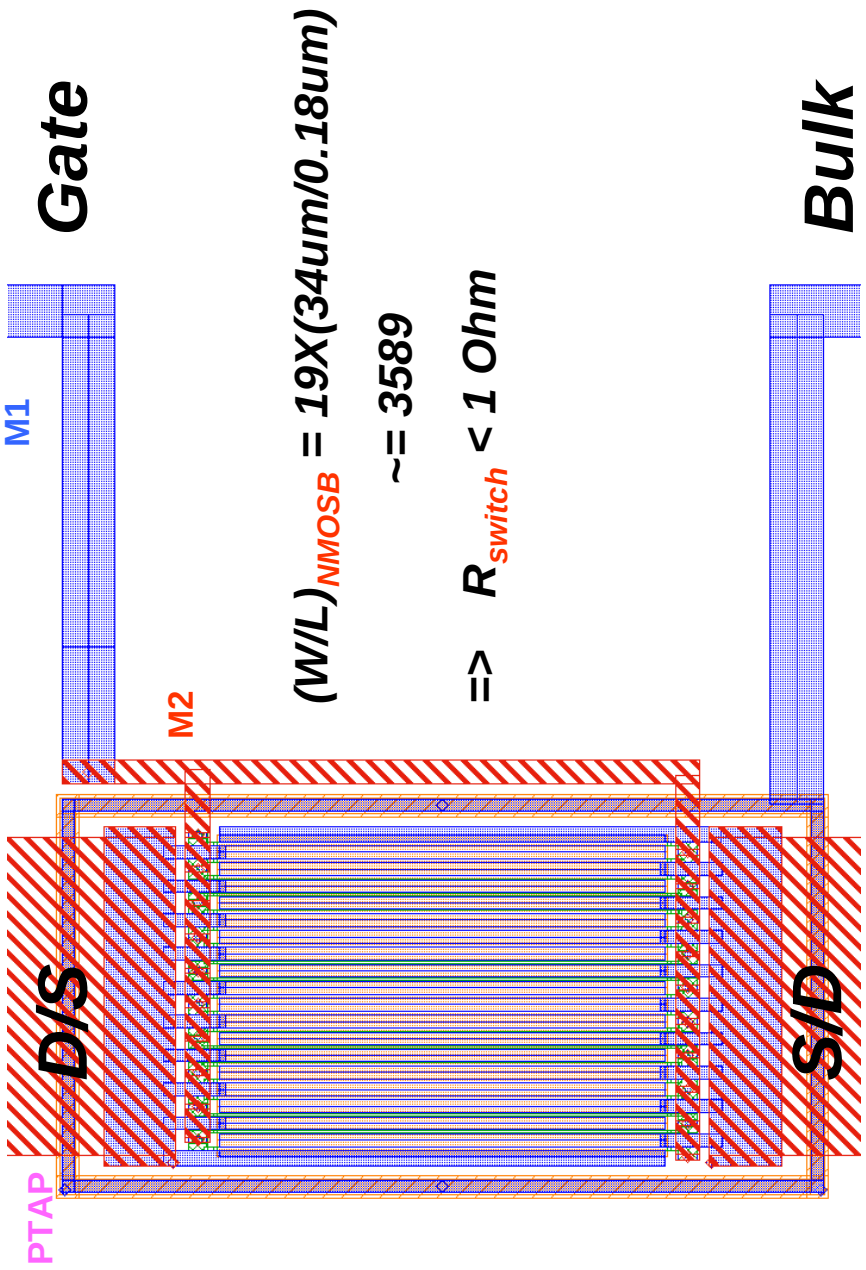


Figure 25: Switch layout for the tunable discrete inductor design.

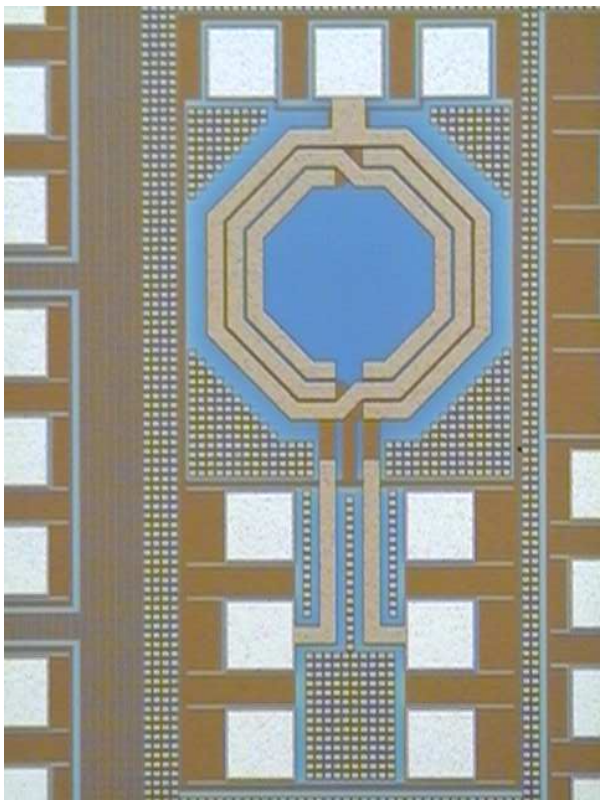


Figure 26: Die microphotograph for the tunable discrete inductor design.

5. Die photo taken by WinTV32

6. VNA - HP8510C

The s-parameter plots after LRRM calibration are shown in Figure 27. From these plots, we find that s11 and s22 are well below -70 dB and s12 and s21 are well within ± 0.002 dB, indicating that we have obtained an excellent calibration. Therefore we can move on to the on-wafer probing measurements. The measurement results are shown in Figure 28. It is obvious that the inductance is indeed reduced by about a half when the switch is on.

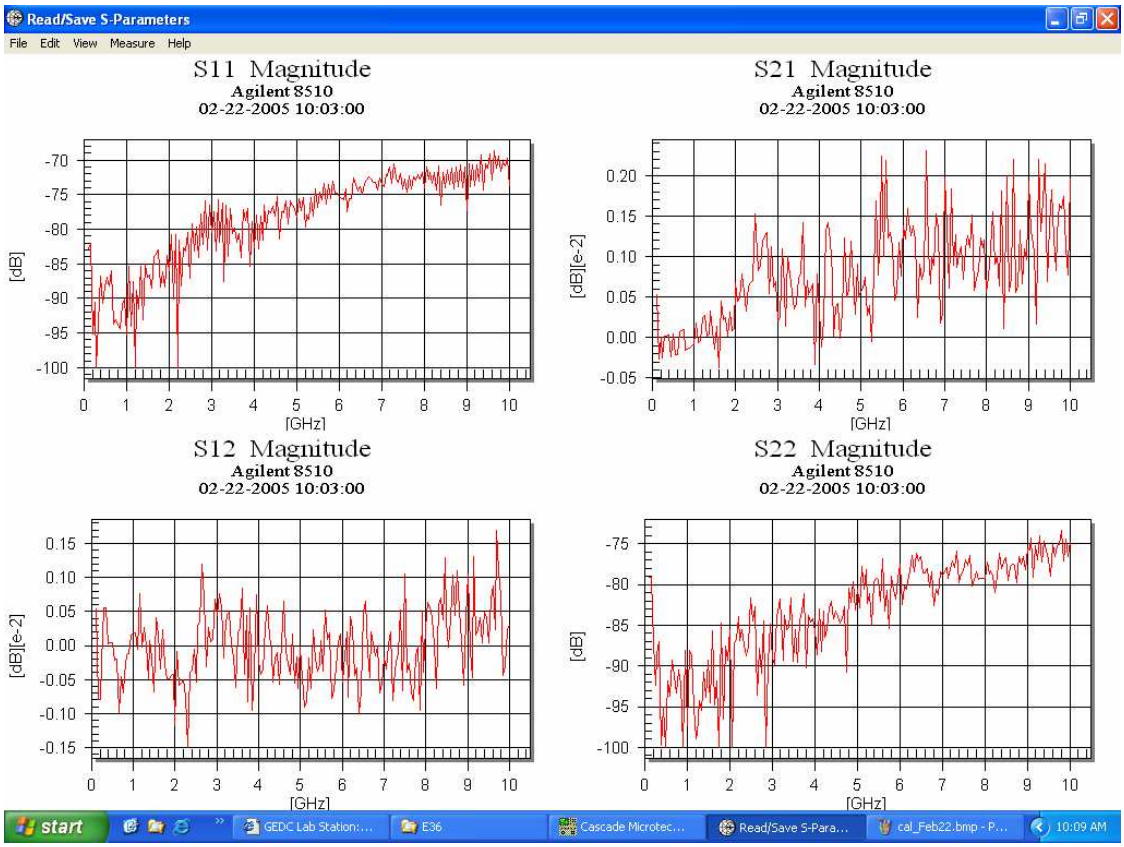
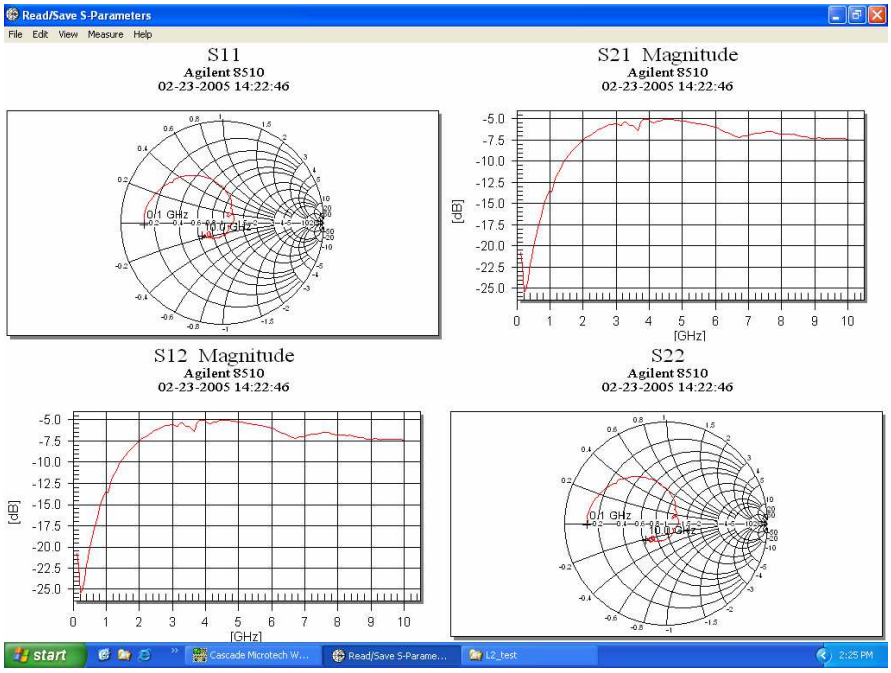
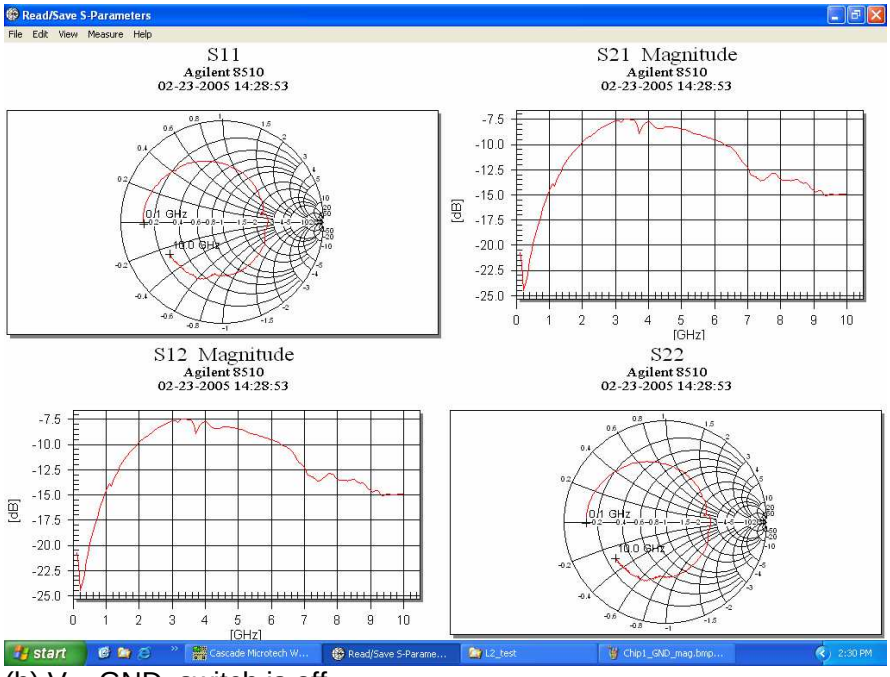


Figure 27: LRRM calibration results for on-wafer probing test.



(a) V_G=VDD, switch is on



(b) V_G=GND, switch is off

Figure 28: On-wafer probing measurement results for the tunable discrete inductor design.

3.2 On-chip capacitors

3.2.1 Introduction to on-chip capacitors

On-chip capacitors include both fixed capacitors and variable capacitors (i.e. varactors). For the on-chip fixed capacitors, Q, capacitance/area ratio, and linearity are the most important parameters. Other parameters such as voltage and temperature coefficients etc will also become important in some special applications. Parasitic capacitances from both terminals of the desired capacitance to the ac ground are also something that we need to be aware of when doing the design. For the varactors, there are two more important parameters: C_{max}/C_{min} ratio (the tuning range) and $K_{VC,max}/K_{VC,min}$ (the tuning linearity with the control voltage).

Fixed capacitors can be implemented by either MOS capacitors (polysilicon-oxide-polysilicon/poly-poly, poly-to-n-well, etc.) or metal-insulator-metal (MIM) capacitors. MIM capacitors include the conventional MIM capacitors, the standard horizontal-parallel-plate (HPP) structure capacitors, the vertical-parallel-plate (VPP) structure capacitors, and the vertical-bar (VB) structure capacitors. Generally speaking [5, 6, 18], MOS capacitors, especially the poly-poly, suffer much lower Q but have higher density. They are typically used for power supply ripple by-passing and applications where the area is more important or the operating frequency is low. MIMs, on the other hand, have the highest Q but lower density. The VPPs and VBs have comparable Q and $\sim 20\%$ higher density, better matching, and higher SRF than the conventional MIMs and HPPs [3]. An EM simulator has to be used to design those MIM capacitors due to the lack of closed-form formula.

To achieve higher Q, varactors using electrons as major carriers are preferred. This leads to the following three main CMOS-compatible varactor structures:

1. The p-n junction diode (for example, p^+-to-n-well).

2. The NMOS-based capacitor operated in inversion mode only (I-mode NMOS-based varactor). It has a monotonic C-V relation.

3. The NMOS-based capacitor operated in accumulation mode only (A-mode NMOS-based varactor). It also has a monotonic C-V relation.

They are illustrated in Figure 29.

In addition to the above three varactors using electrons as major carriers, the I-mode PMOS-based varactor, even with less Q due to using holes as major carriers, is still another popular choice. This is because we can get an extra control by changing the NWELL biasing voltage in the NWELL technology. Also the NWELL of PMOS provides some shielding, which is desirable in the mixed-signal design.

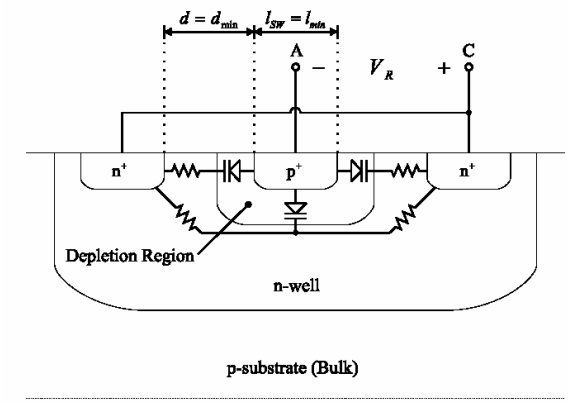
Performance comparison of these types of varactors can be found in [42] [45]. From the experimental data, the following observations are formed:

1. The p^+-to-n-well junction varactor has the highest Q; even with 0.5-μm technology, a Q higher than 100 is achievable. For a MOS capacitor based varactor, the Q is typically less than 50.

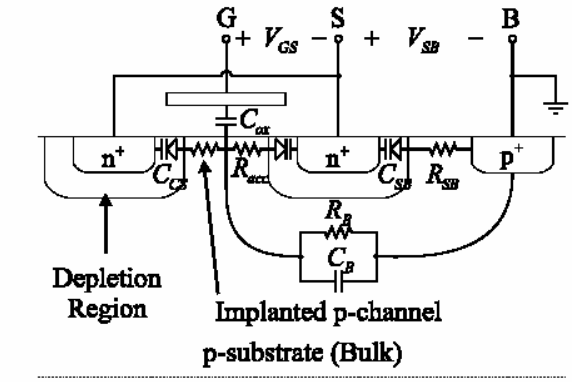
2. On the other hand, the p^+-to-n-well junction varactor has the lowest C_{max}/C_{min} ratio, typically less than 2. Hence, it has the smallest tuning range. MOS capacitor-based varactors usually can have a C_{max}/C_{min} larger than 2, even 3 possibly.

3. For linearity, a MOS capacitor-based varactor usually has much larger $K_{VC,max}/K_{VC,min}$ than a junction diode varactor and hence less linear frequency tuning characteristic.

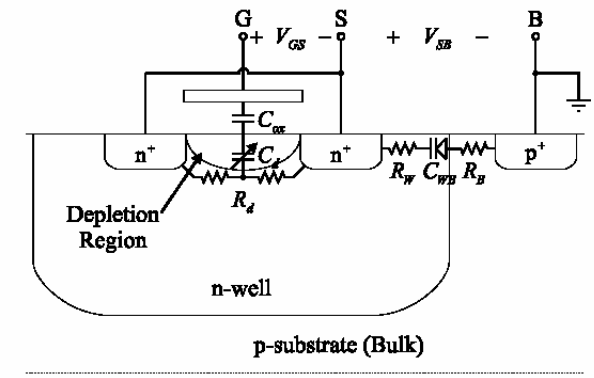
This section is organized as follows. The measurement results for a fabricated 1 pF CPP is presented in Section 3.2.2. The new TDC idea is presented in Section 3.2.3.



(a) P+-to-n-well junction varactor



(b) Standard mode NMOS



(c) Accumulation mode NMOS

Figure 29: Three types of varactors using electrons as major carriers

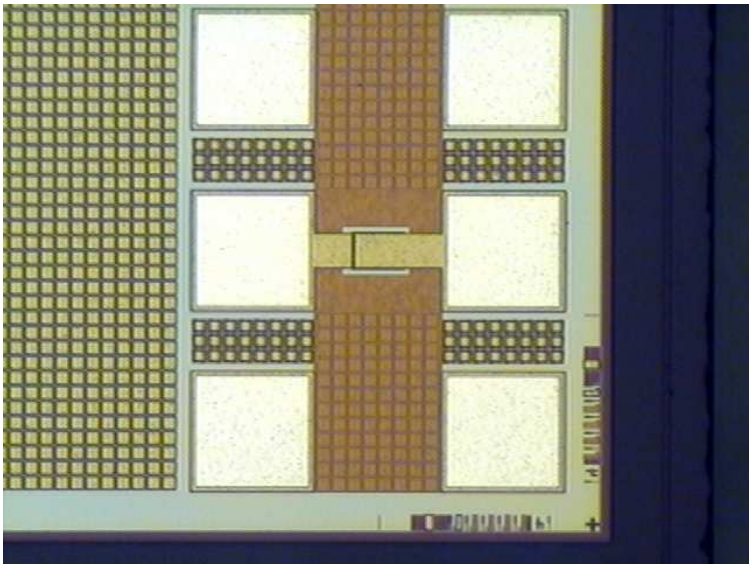


Figure 30: Die microphotograph for a fabricated 1 pF CPP.

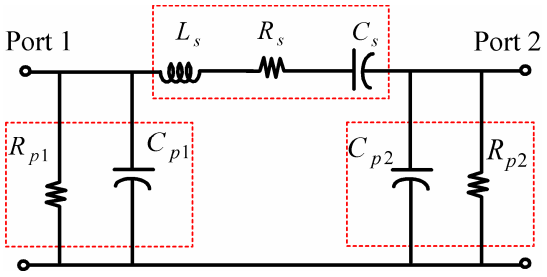
3.2.2 Poly-poly capacitors

The die microphotograph for a fabricated 1 pF CPP is shown in Figure 30. The electrical model with lumped elements and the extracted values are shown in Figure 31. The measured s-parameter before and after two-step deembedding and the s-parameter from the extracted electrical model are shown in Figure 32 (only s22 included, the others have the same similarities.).

It can be seen from the above results that the CPP is very well simulated in Cadence and easy to design with a good tolerance. The bottom plate of CPP usually has an around 12% parasitic capacitance while the top plate's parasitic capacitance is usually negligible.

3.2.3 Tunable Discrete Capacitor (TDC) using I-mode varactors

One copy of TDC is illustrated in Figure 33. The key idea is instead of operating I-mode PMOS based varactor in the middle sharp continuous range, we bias it in a way that only uses the on- and off-state. Consequently, a two-level capacitance is obtained [50]. It has a much smaller capacitance variation over a much wider range.



R_S	12.1439 Ohms
L_S	17.3573 pH
C_S	1.0207 pF
R_{P1}	2.6331 KOhms
C_{P1}	113.7356 fF
R_{P2}	578.7842 KOhms
C_{P2}	2.0942 fF

Figure 31: The extracted lumped electrical model for the fabricated 1 pF CPP

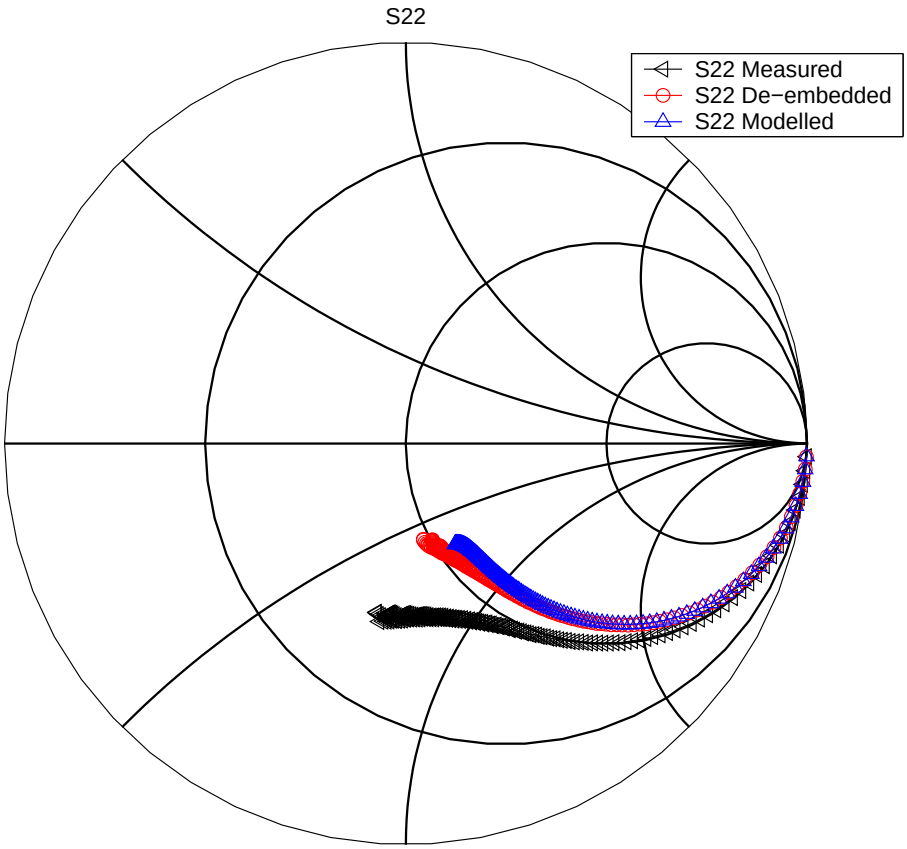


Figure 32: The s-parameter plots for the measured s-parameter before and after two-step deembedding and the s-parameter of the extracted lumped electrical model for the fabricated 1 pF CPP

The new designs here are:

(1) Two DC biasing voltage $VS1$ and $VS2$ are connected through four 1 $M\Omega$ n-well resistors to the four I-mode varactors to compensate the threshold voltages needed to form inversion layers. I.e. $VS1$ and $VS2$ shift the sharp transition region to the middle of rail-rail voltage.

(2) Four high-linearity, equal-value, fixed capacitors are connected in series with the I-mode varactors to further expand the allowable signal swing.

(3) Q_ctl1 and $Q\_ctl1Bar$ are two complementary digital control signals either $0V$ or $1.8V$. They are converted to smaller two-level digital voltages, either $0.35V$ or $1.45V$ via the inverter+diode-connected active loads. This ensures that TDC is biased at the middle voltage of each capacitance level, hence allows the maximum ac swing.

(4) We use two complementary copies by flipping the G/DS connections of I-mode varactors to compensate the small capacitance variation slope mainly due to the gate depletion width changes, hence an improved linearity is achieved during ac signal swing.

Figure 34 shows the simulation results of 3-bit TDC design. Both ac and transient simulation reveal a similar behavior. In reality, there will be some variations due to finite Q of each element.

3.3 Summary

In this chapter, we first present the common practices for high Q inductor design. Then a new idea to design tunable discrete inductor is explained with measurement results. The later half of this chapter is devoted to the on-chip capacitors including both fixed and variable capacitors. One poly-poly capacitor is fabricated and measured. The idea of designing a tunable discrete capacitor is presented last with simulation results.

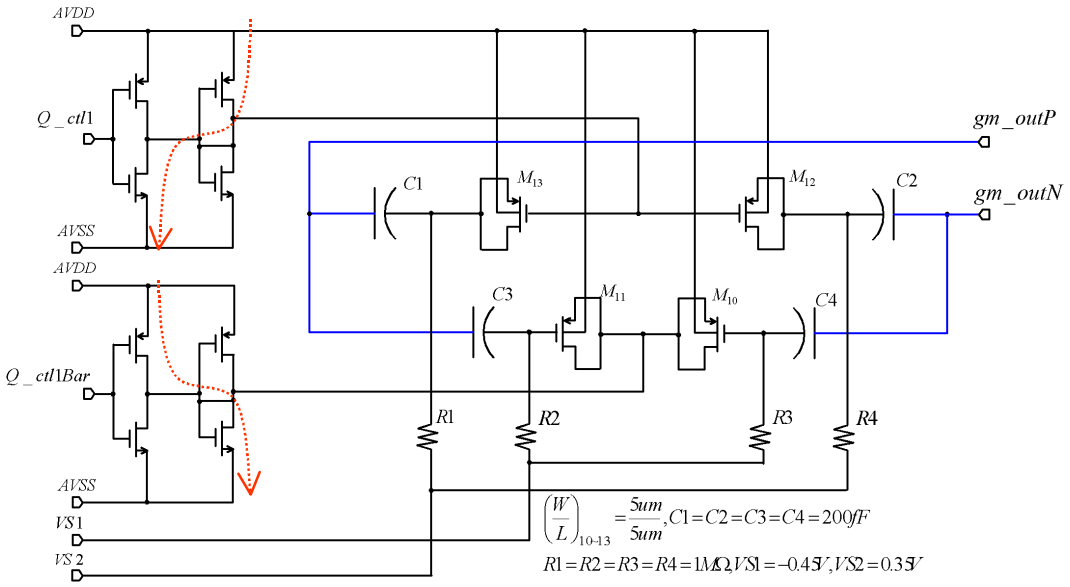


Figure 33: One copy of Tunable Discrete Capacitor.

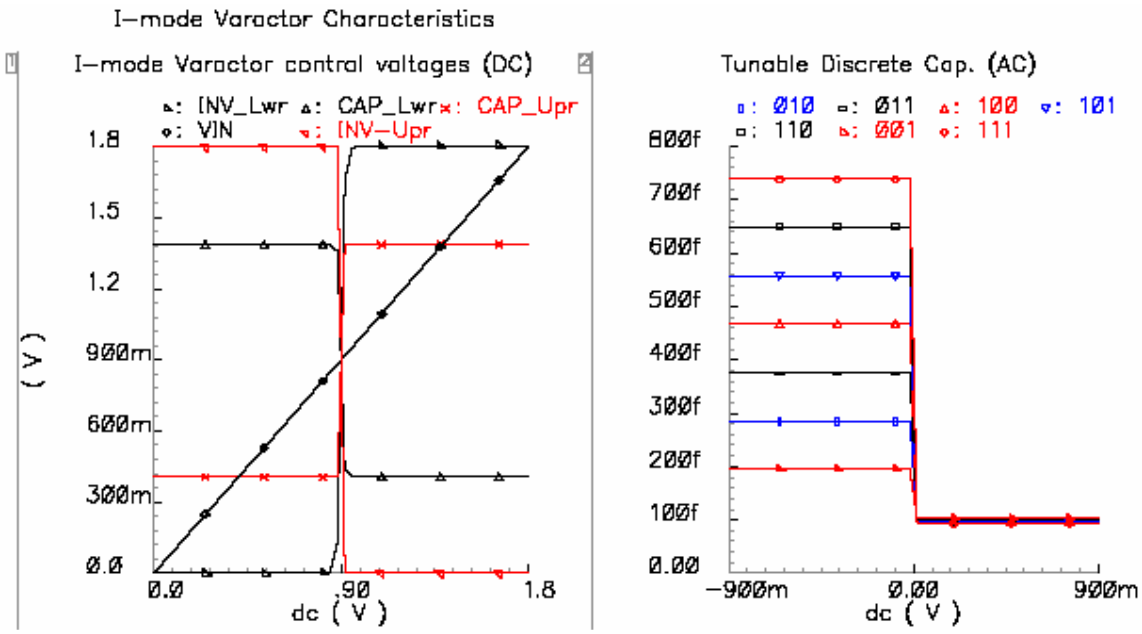


Figure 34: Simulation Results of TDC.

CHAPTER 4

CMOS RF ON-CHIP FILTERS USING ONE Q-ENHANCED LC TANK [32]

As we have explained in Chapter 1, in order to replace those off-chip RF filters while having an acceptable DR performance, we need use Q-enhanced LC filters instead of the G_m-C filters due to the passive inductor's energy-storage capability instead of active inductor's energy-dissipation property. Generally speaking, with inductor's quality factor to be Q_0, Q-enhanced LC filters can have an up to Q_0^2 times better DR than G_m-C filters.

Since the first use of on-chip inductor for RF LC filters design [39], consistent efforts have been found [13, 30, 37, 49] to improve LC filters' performance. Theoretically [27], an LC filter can achieve a comparable DR performance as the current off-chip ceramic and/or SAW filter solution with the upper limit given in (29).

$$\frac{Q}{Q_0} \sim\leq \sqrt{\frac{FG}{4(\gamma+1)}} \tag{29}$$

where Q is the desired filter quality factor, Q_0 is the achievable inductor quality factor, F is the noise factor, G is the power gain, and γ is the noise parameter.

In reality, due to the nonlinearity introduced by the negative resistance for loss compensation, the varactor for frequency tuning, and the input OTA for gain control, the P1dB is usually limited to only -10 dBm or so with deep-submicron technologies. This not-so-good linearity basically limits the DR.

In this chapter, a divide-and-conquer method is presented to improve the overall system linearity while keeping the high dynamic range based on the overall system as shown in Figure 35. First, the theoretical analysis of the one Q-enhanced LC

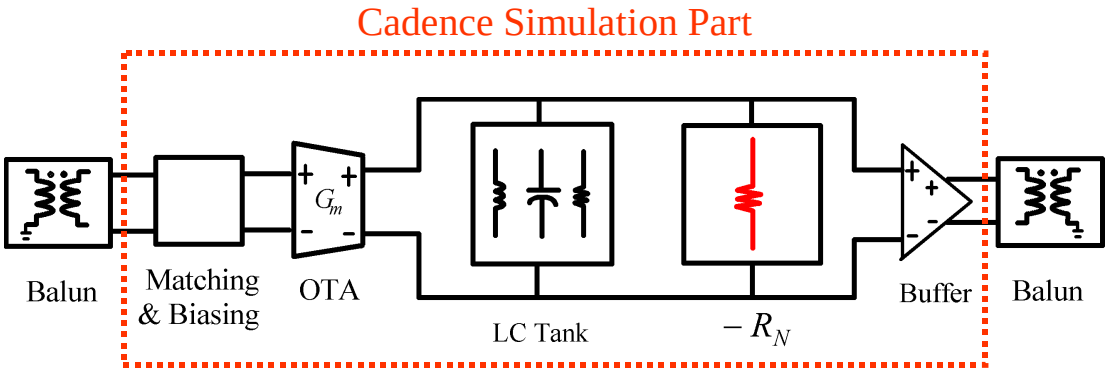


Figure 35: Overall filter system with Q-enhanced LC tank.

tank BPF is introduced in Section 4.1 to provide some design guidelines. Second, the building blocks are described in Section 4.2. Last, two simulation cases corresponding to the lowest-end and highest-end frequency of the wireless and data communication standards [43] are presented in Section 4.3 to verify the performance and frequency handling capability of the new design.

4.1 Theoretical analysis of one Q-enhanced LC tank BPF

In order to simplify the analysis, we will first present in Section 4.1.1 the simplified model for one Q-enhanced LC tank BPF used in our derivations.

4.1.1 Simplified model for one Q-enhanced LC tank BPF

With the narrow-band equivalent models for on-chip inductor (for example, differential structure, octagonal shape with center tap ac ground) and capacitor (poly-poly capacitor) introduced in Chapter 3 and conversion between series and parallel RLC networks [29], the following simplified narrow-band model for LC tank can be obtained as shown in Figure 36.

And using a simple negative resistor resulting from the g_m-based negative resistance generation mechanism and a simple G_m for input OTA, we can get the following

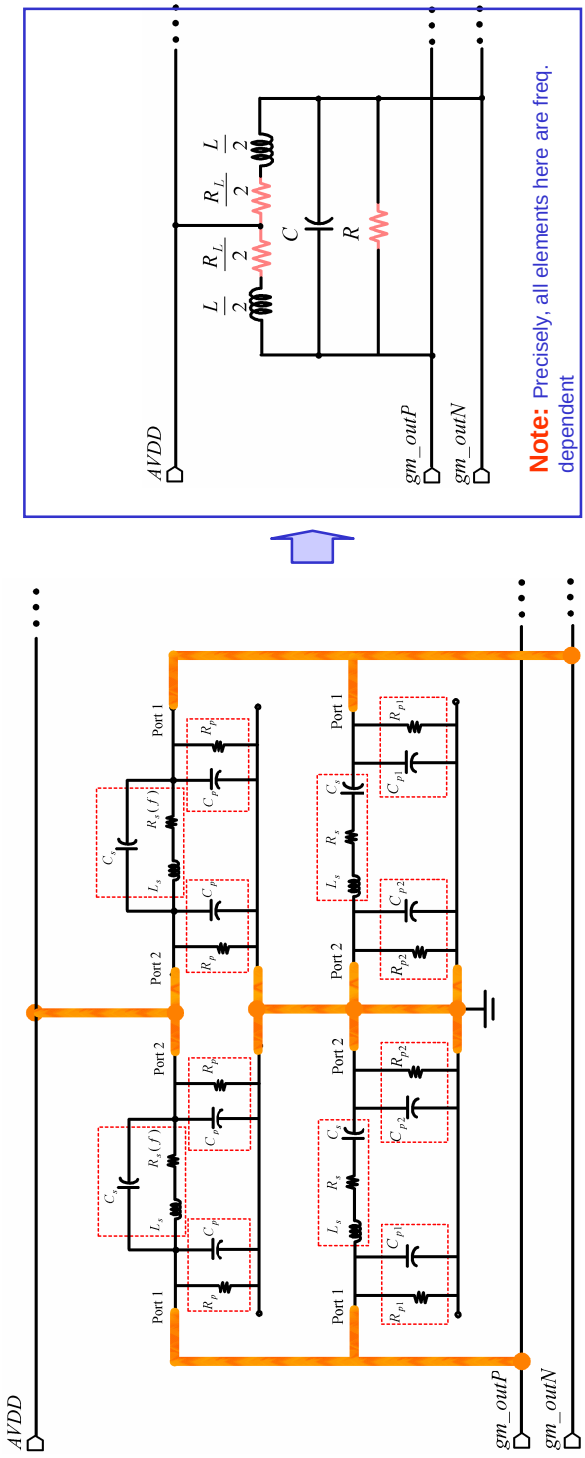


Figure 36: Simplified narrow-band model for LC tank.

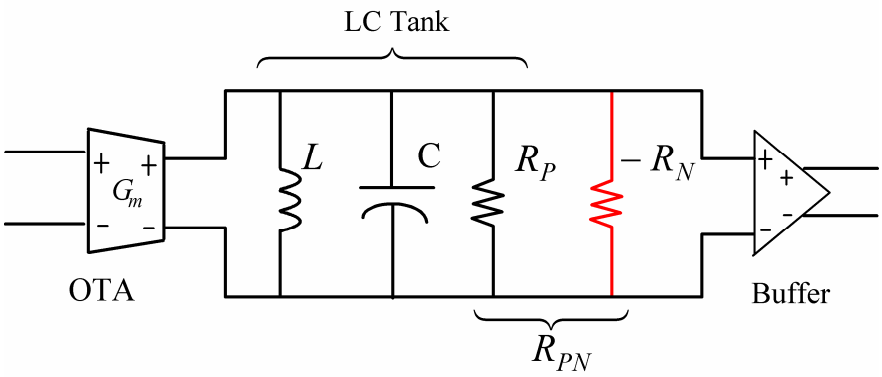


Figure 37: Simplified model for one Q-enhanced LC tank BPF.

simplified model for one Q-enhanced LC Tank BPF as shown in Figure 37.

4.1.2 Ideal parallel compensation of LC tank without center frequency shifting

The simple LC tank with parallel loss compensation by R_N is shown in Figure 38. Inductor L's loss is modeled by a simple series resistor R_L. The objective here is to achieve a quality factor of Q at resonant frequency ω_0. The voltage transfer function is given in (30). There are two requirements or knowns (the desired resonant frequency and Q) and two control variables or unknowns (negative resistance R_N for Q and either reduced inductance or capacitance for ω_0), so the solution is unique. The two methods are illustrated in Figure 39 and the corresponding solutions are given in Table 7. A simple example with L of 5 nH, RL of 5.5386 Ω, and C of 5.9568 pF is simulated to verify the above two methods as shown in Figure 40.

$$V_L = \frac{\frac{(R_L+SL)}{L}V(0)}{S^2 + S\left(\frac{R_L}{L} + \frac{1}{R_N C}\right) + \left(1 + \frac{R_L}{R_N}\right)\frac{1}{LC}} = \frac{\frac{(R_L+SL)}{L}V(0)}{S^2 + S\frac{\omega_0}{Q} + \omega_0^2} \tag{30}$$

4.1.3 Sensitivity analysis and synchronous tuning of f_0, gain, and Q

Synchronous tuning of f_0, gain, and Q means that when the filter Q is digitally tuned to meet different selectivity/DR [27] requirements by changing g_{mN} $(= -1/R_N)$ for a

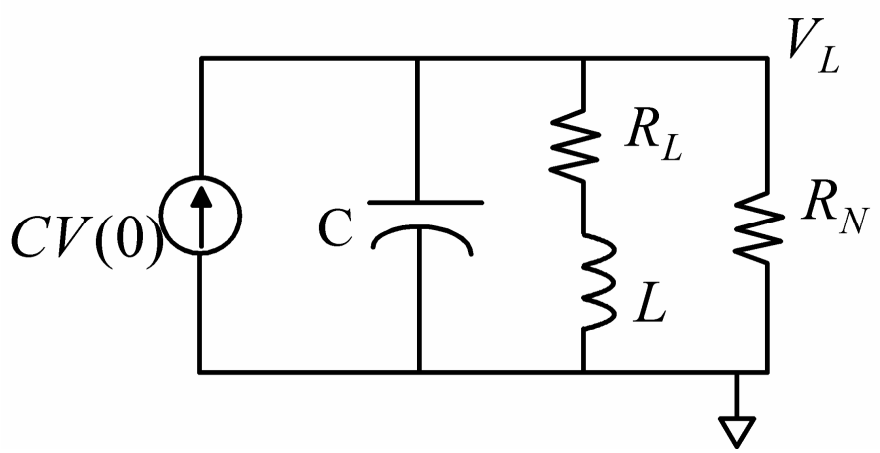
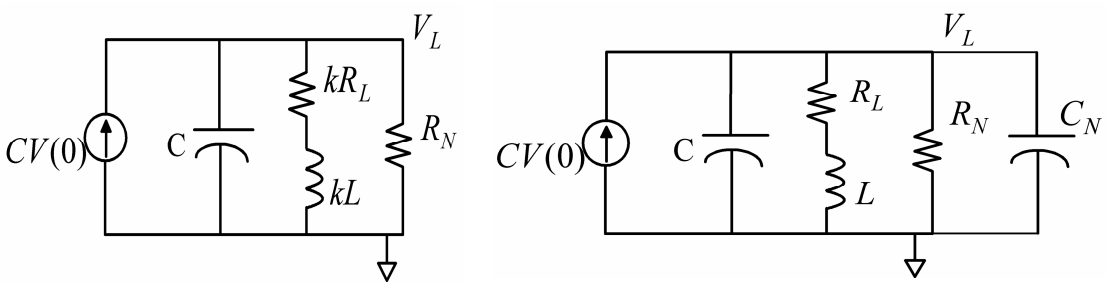


Figure 38: Simple LC tank with parallel compensation.



(a) Reduced L + R_N (b) Reduced C + R_N

Figure 39: Two parallel compensation methods for simple LC tank.

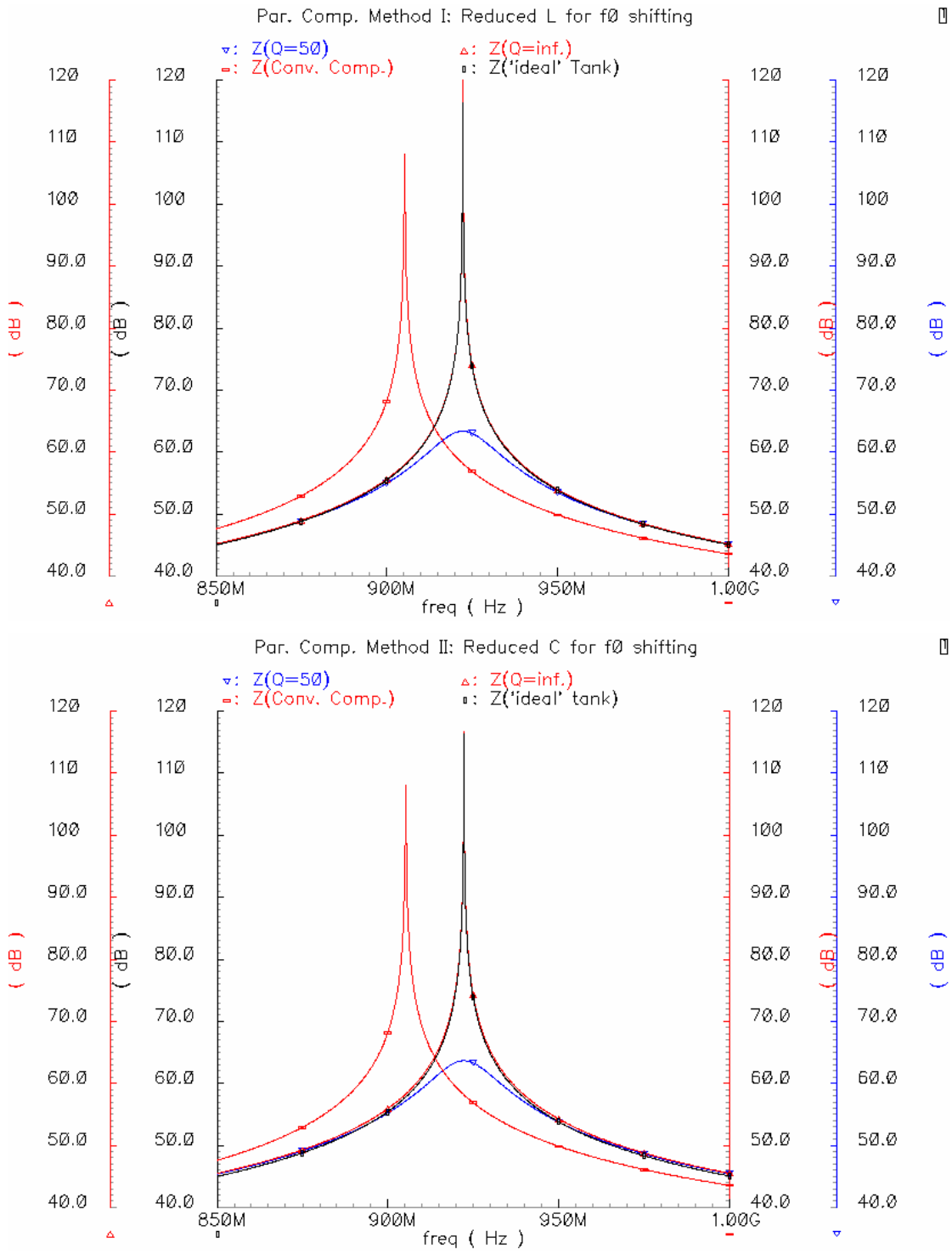


Figure 40: Simulation results to verify the two parallel compensation methods.

Table 7: Two Solutions for Parallel Compensation.

Method I:Reduced $L + R_N$	**Method II:Reduced** $C + R_N$
$R_N = \frac{1}{(\frac{\omega_0}{Q} - \frac{R_L}{L})C}$	$R_N = -R_L + \frac{1}{(\frac{\omega_0}{Q} - \frac{R_L}{L})C}$
$k = \frac{R_N}{R_N - R_L}$	$C_N = C\frac{(R_N - R_L)}{R_N} - C = -C\frac{R_L}{R_N}$

given g_{mP} $(= 1/R_P)$ of equivalent LC tank loss, the center frequency should not drift and the gain should also be kept constant.

By observing some simple relations (31) and (34) among Q, gain, and tunable variables, such as G_m of input OTA and g_{mN} of negative resistance, we can derive the sensitivities of filter Q and gain w.r.t. g_{mN} and G_m assuming a -3 dB gain.

With

$$Q = \frac{\omega_0 C}{g_{mP} - g_{mN}} \tag{31}$$

we have:

$$S^{Q}_{g_{mN}} = -S^{g_{mP}-g_{mN}}_{g_{mN}} = \frac{g_{mN}}{g_{mP} - g_{mN}} \tag{32}$$

With

$$Gain = \frac{1}{2} = \frac{1}{2} G_m R_{PN} = \frac{1}{2} \frac{G_m}{g_{mP} - g_{mN}} \tag{33}$$

we have:

$$G_m = g_{mP} - g_{mN} \tag{34}$$

i.e. G_m is inverse proportional to g_{mN}. And

$$S^{Gain}_{g_{mN}} = -S^{g_{mP}-g_{mN}}_{g_{mN}} = \frac{g_{mN}}{g_{mP} - g_{mN}} \tag{35}$$

The graphic illustrations of filter Q and sensitivity of Q v.s. g_{mN} are shown in Figure 41. These transcendental relationships intuitively explain:

1. Why the 1-dB gain compression point is inversely proportional to the filter Q.
2. Why the tuning at high filter Q is very difficult.
3. Why the high Q filter is prone to oscillation. etc.

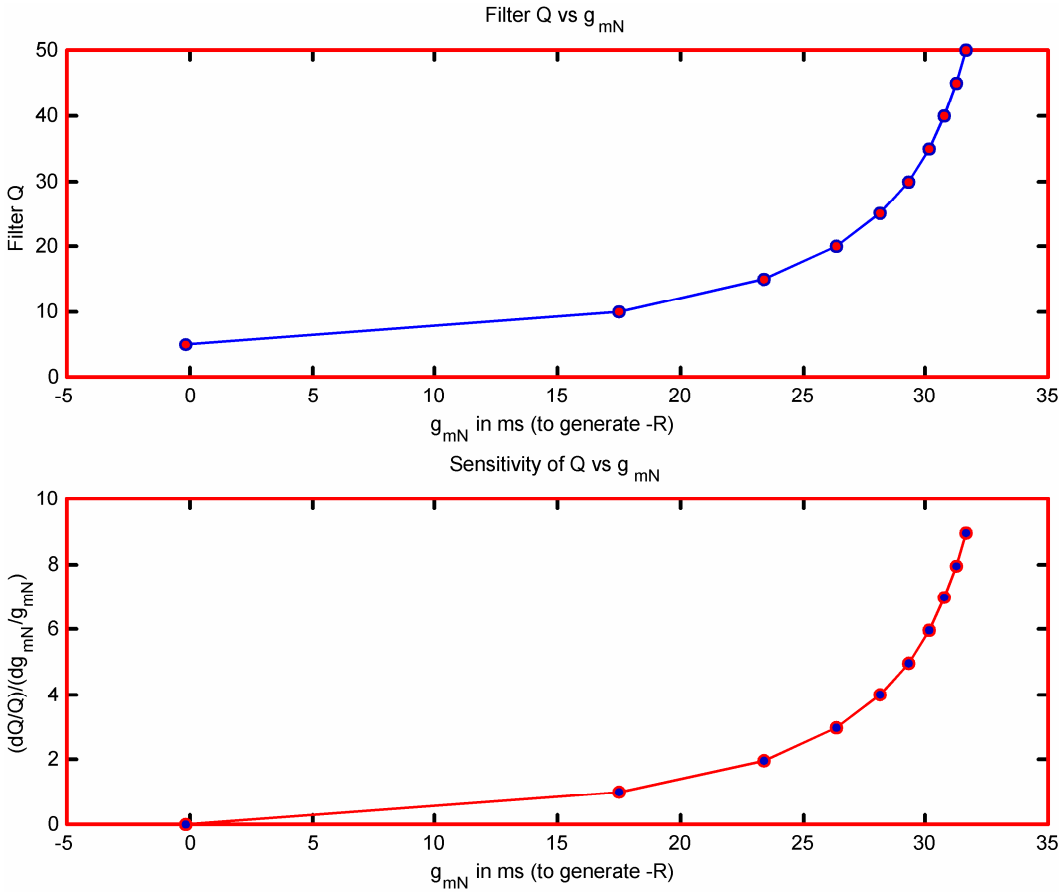


Figure 41: Filter Q and sensitivity of filter Q v.s. g_{mN} of -R.

The inverse proportional relation between G_m of the input OTA and g_{mN} of loss compensation negative resistance can be implemented via some inverters between their controlling signals. For example, suppose that g_{mN} is decreased for lower Q, then G_m should be increased to keep the gain constant. The center frequency shifting is mainly due to switching in and out some g_{mN} cells when we tune the filter Q. This can be compensated by adding a corresponding amount of capacitance, which, for example, can be the new wide-range and high-linear TDC circuit introduced in Chapter 3.2.3. In this way, we can achieve the synchronized coarse tuning of f_0, gain, and Q. The fine tuning can be done in the following steps by considering the weak interaction among f_0, gain, Q, and the control variables such as G_m and g_{mN}:

1. Tune C for f_0 fine tuning. This can be done using a phase locked loop (PLL).
2. Tune g_{mN} for fine filter Q tuning. The Q can be detected using some shape detector circuit that helps to control the g_{mN}.
3. Tune G_m for fine gain tuning. The gain can be detected with some peak detector circuit that helps to control the G_m.

4.1.4 Noise analysis

The simplified circuit for noise analysis of one Q-enhanced LC tank BPF is shown in Figure 42. Using the thermal noise model for both MOS transistor and resistor and flicker noise model for transistor [2], we can calculate the total input-referred noise in (36). Notice that the thermal noise is in a form of kT/C, which indicates that picking larger inductance will potentially result in a noisier circuit.

$$\begin{aligned}\overline{v}_{n,in}^2 &= \overline{i}_{n,out}^2 B_n / G_m^2 \\ &= 2 \times \frac{kT}{C}\frac{1}{R_{PN}}\frac{1}{G_m^2}\left[\frac{(g_{mN}+G_m)(1+\eta)}{3}+\frac{2}{R_P}\right] \\ &+ 2 \times \frac{K_{FN}}{G_m^2 C_{OX}^2}\left[\int_{f_{-3dB}}^{f_{+3dB}} \frac{g_{mN}^2}{(WL)_{g_{mN}}}\frac{1}{f^n}df + \int_{f_{-3dB}}^{f_{+3dB}} \frac{G_m^2}{(WL)_{G_m}}\frac{1}{f^n}df\right]\end{aligned} \tag{36}$$

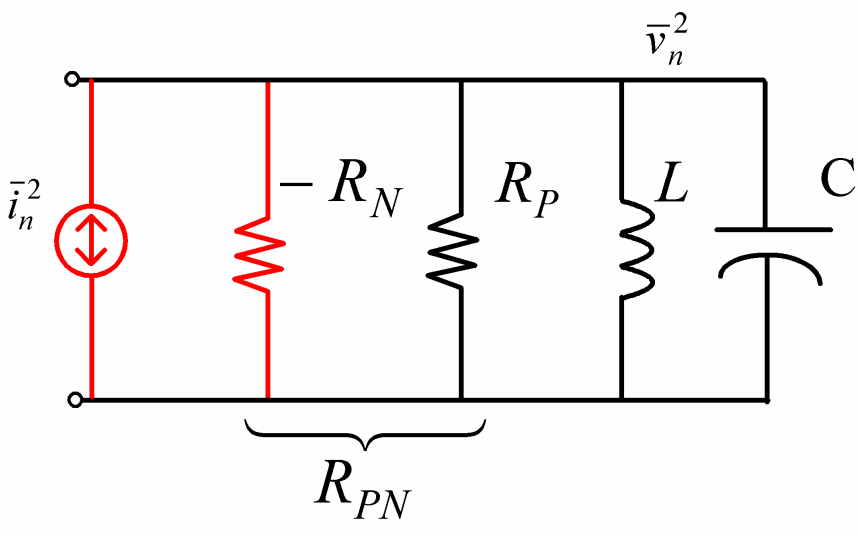


Figure 42: Simplified circuit for noise analysis.

The noise spectrum for the MOS transistors used in this project can be obtained via some simple simulation circuits. It is shown in Figure 43.

Using the curve-fit toolbox available in $MATLAB$®, we can extract the noise parameters as illustrated in Figure 44. The extracted noise parameters for the NMOS are as follows:

$$\eta \approx 1.29 \tag{37}$$

$$n \approx 0.7794 \tag{38}$$

$$K_{FN} \approx 3.8895 \times 10^{-26} \sim C^2/M^2 \tag{39}$$

A $MATLAB$® script is written with the above parameters and the total input-referred noise formula in (36) to predict the circuit's noise performance, which, not surprisingly, is usually within 2% error compared with what Cadence simulates.

4.1.5 P1dB analysis

The simplified circuit for 1 dB compression point analysis of one Q-enhanced LC tank BPF is shown in Figure 45.

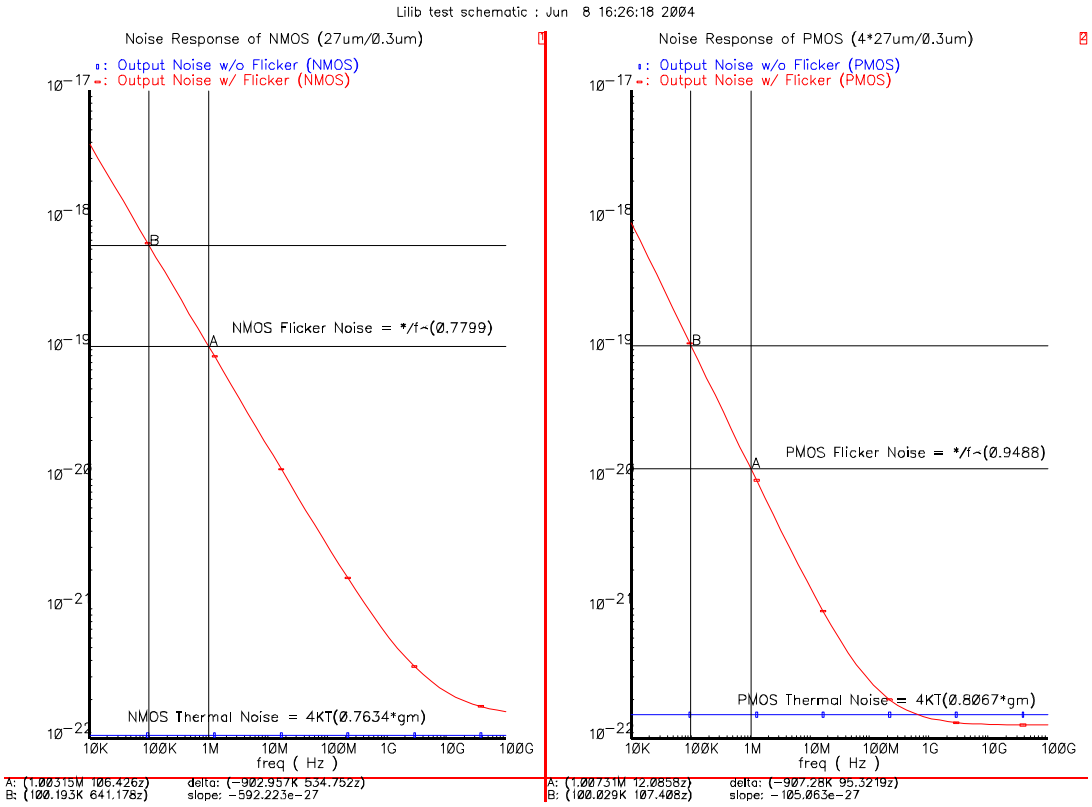


Figure 43: NSC's CMOS transistors' flicker and thermal noise simulation results.

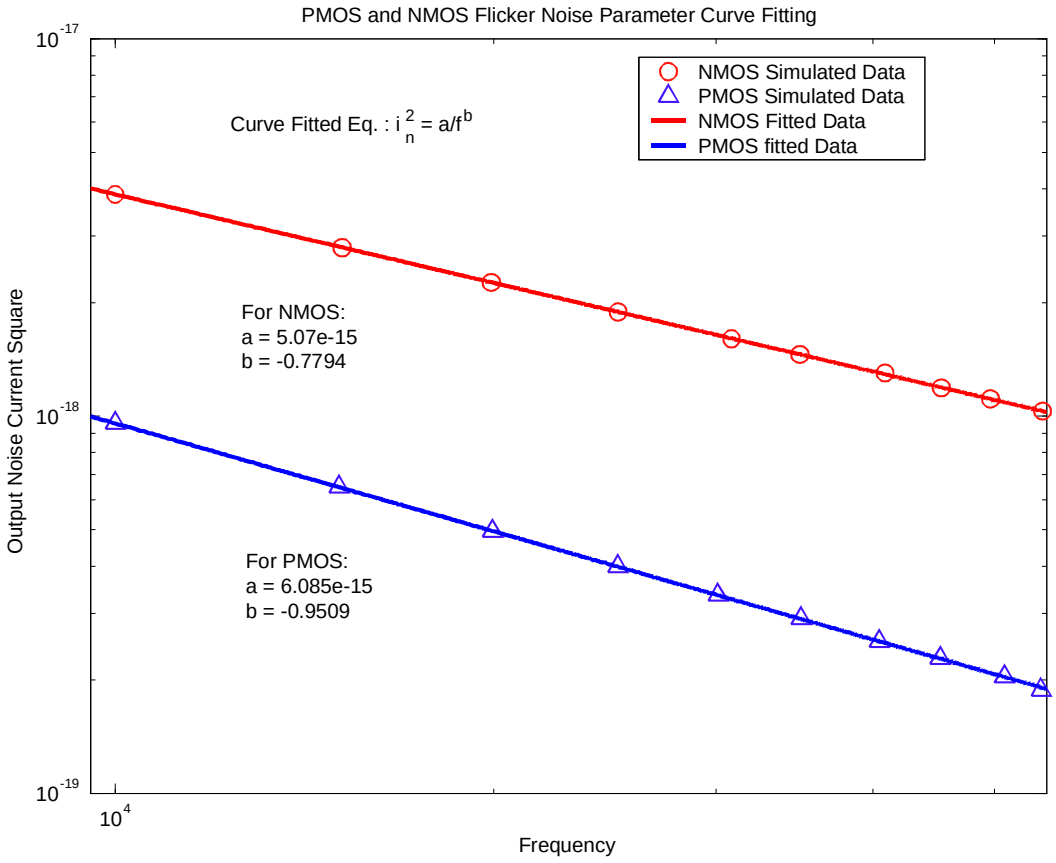


Figure 44: Curve-fit for nMOS flicker noise parameters extraction.

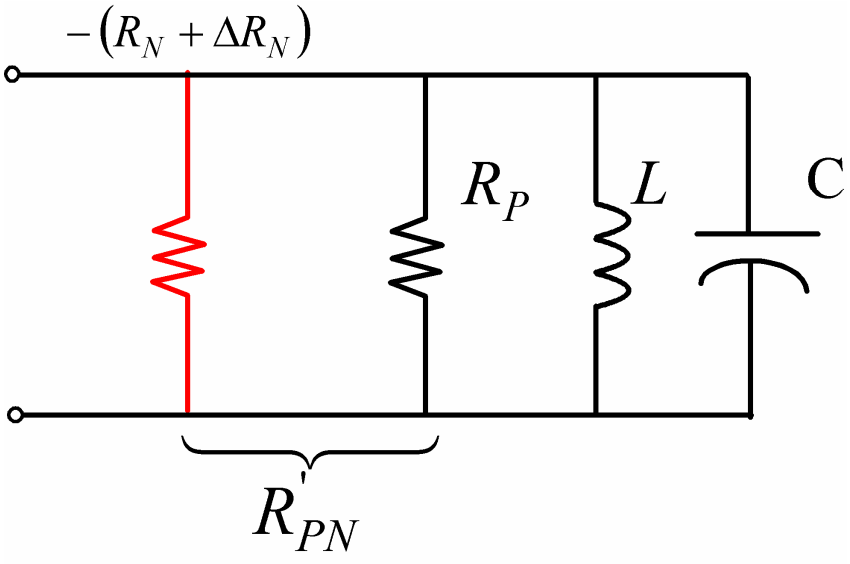


Figure 45: Simplified circuit for 1 dB compression point analysis.

Where:

$$R_{PN} = (-R_N)//R_P = \frac{R_N R_P}{(R_N - R_P)} \tag{40}$$

$$\begin{aligned} R'_{PN} &= (-(R_N + \Delta R_N))//R_P \\ &= R_{PN}\frac{R_N R_P}{(R_N - R_P)} = R_{PN}\frac{1 + \frac{\Delta R_N}{R_N}}{1 + \frac{\Delta R_N}{(R_N - R_P)}} \end{aligned} \tag{41}$$

By neglecting the non-linearity from the input OTA, tank C, and output buffer, we can calculate the 1 dB compression point in (42).

$$\begin{aligned} &20\log_{10}\left\{\frac{A'_v}{A_v}\right\} = 20\log_{10}\left\{\frac{R'_{PN}}{R_{PN}}\right\} = -1 \\ &\Rightarrow \frac{R'_{PN}}{R_{PN}} = \frac{R_N R_P}{(R_N - R_P)} = R_{PN}\frac{1 + \frac{\Delta R_N}{R_N}}{1 + \frac{\Delta R_N}{(R_N - R_P)}} \approx 0.8913 \approx \frac{9}{10} \\ &\Rightarrow \frac{\Delta R_N}{R_N} = \frac{R_N - R_P}{10R_P - R_N} \end{aligned} \tag{42}$$

For a filter Q of 45 at 900 MHz, with inductor Q of 5, the P1dB can be calculated to be $\sim$ 1.35%, indicating a very stringent linearity requirement on the negative resistance.

4.1.6 HD3 and mismatch analysis

Using square-law model and assuming a conventional cascode input OTA, we can calculate the HD3 in (43). The input-referred offset due to the mismatch is given in (44). It is clear that there is a tradeoff between HD3 and mismatch. For example, larger overdrive results in lower distortion but higher offset. Mismatch is important because it

1. Creates DC offsets,

2. Reduces the CMRR, and

3. Deteriorates the even order harmonic distortion suppression.

Also because of the random nature of the mismatch, the offset can be treated as a very low frequency noise. Hence any offset cancelation technique will also reduce the low frequency noise such as flicker noise.

$$HD3 = \frac{1}{32}\frac{v_{id}^2}{(V_{GS}-V_T)^2} = \frac{1}{64}\left(\mu C_{OX}\frac{W}{L}\right)\frac{v_{id}^2}{I_D} \tag{43}$$

$$V_{OS,in}^2 = \left(\frac{V_{GS}-V_T}{2}\right)^2\left\{\left(\frac{\Delta R}{R}\right)^2 + \left[\frac{\Delta(W/L)}{(W/L)}\right]^2\right\} + \Delta V_T^2 \tag{44}$$

4.2 Building blocks of one Q-enhanced LC tank BPF

Refer to the overall filter system using one Q-enhanced LC tank shown in Figure 35, the LC tank model has already been explained in Section 4.1.1. The TDC is presented in Section 3.2.3. In Section 4.2.1, the tunable PDP for input OTA along with the input matching and biasing will be presented. The tunable negative resistor will be explained in Section 4.2.2. And finally in Section 4.2.3, the design considerations and effects of output buffer are explained.

4.2.1 Tunable PDP design

One copy of PDP is illustrated in Figure 15. The key idea is to enhance the linearity without using feedback for high speed. The highlighted operating principles are:

1. Two cascode transistors $MC1$ and $MC2$ are used for I/O isolation.

2. Two additional transistors $MR1$ and $MR2$ are biased such that they absorb most of the nonlinearity of the two input transistors $MF1$ and $MF2$. The resulting difference linear currents are taken from output transistors $MC1$ and $MC2$.

3. $MF1$ and $MF2$ are biased at the middle of rail-rail voltages and gates of $MC1$ and $MC2$ are tied to VDD that allows the maximum overdrive for minimum

$HD3$.

One advantage of this cell is a linear relationship between power and W/L and between available g_m and W/L while the biasing voltage remains constant. Hence both power and available g_m are linearly scalable with W/L. Based on this observation, the 3-bit digital tunable PDP can be designed as shown in Figure 46.

In Figure 46, Part 1 is for matching and biasing. A simple linear polysilicon 50 Ω resistor is used for matching instead of inductive source degeneration (ISD) for the following reasons:

1. ISD matching uses more silicon area. That is obvious as on-chip inductors take more silicon area.

2. The inductors used in ISD matching generate magnetic flux, causing more inductive coupling with the other parts of the chip.

3. ISD matching is frequency dependent matching. That is because the real input equivalent 50 Ω is generated from the source inductance, which is frequency dependent. However, 50 Ω resistor is inherently broadband. In addition, for any resistance between $\sim 26\Omega$ and $\sim 96\Omega$, we can get a return loss (RL) better than 10 dB. This wide resistance range usually covers any PVT variation of the 50 Ω poly-resistor.

4. For low frequency application such as GSM-900 MHz, huge gate inductance is needed in ISD matching. This is mainly due to the smaller gate capacitance desired for higher f_T hence better NF.

5. 50 Ω resistor simply contributes negligible noise considering that its noise floor is only -168 dBm/Hz and RF filter noise peak PSD is usually close to that of a 1 KΩ resistor, -155 dBm/Hz.

6. ISD matching design is more complicated.

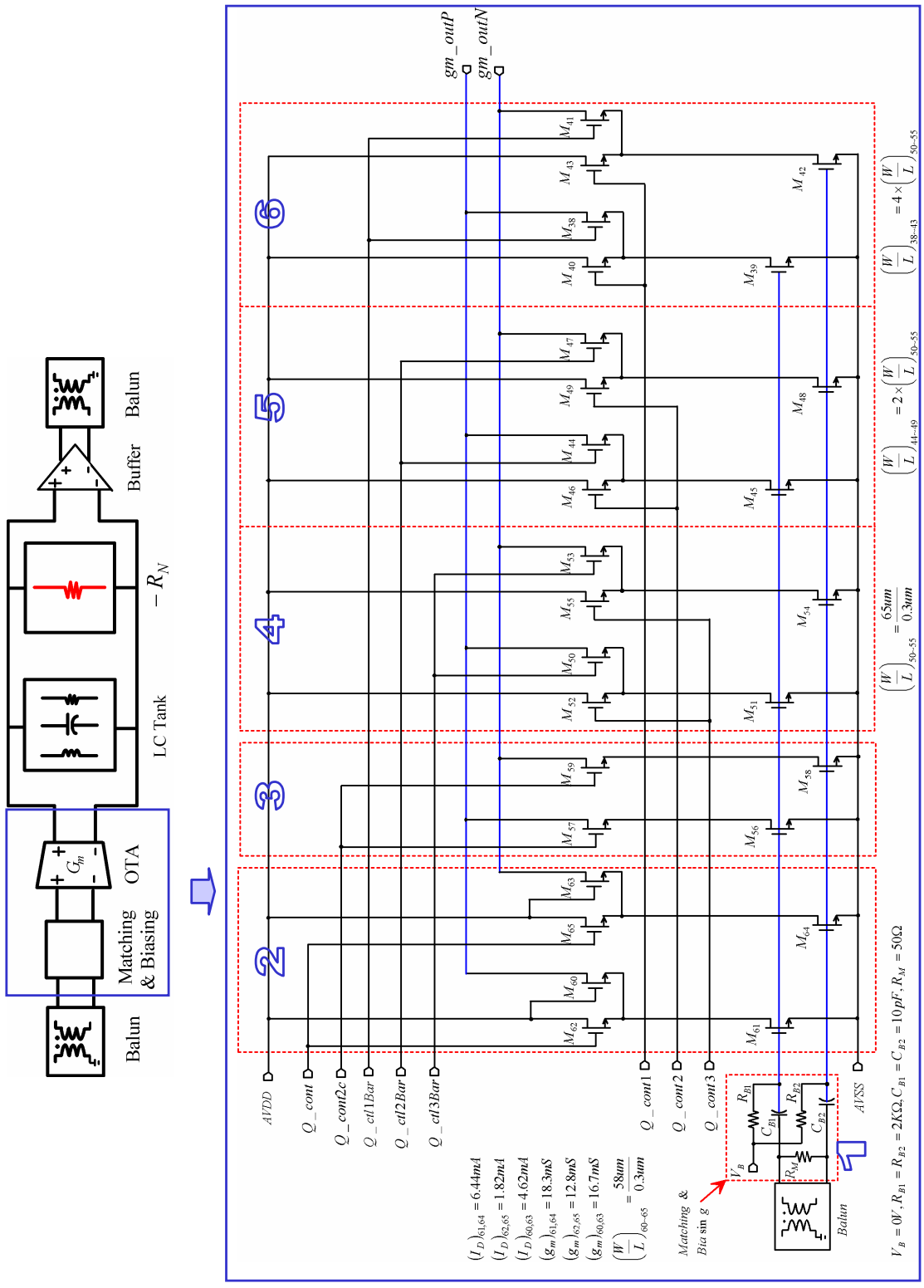


Figure 46: Tunable PDP for input OTA (Parts 1-6 shown on figure)

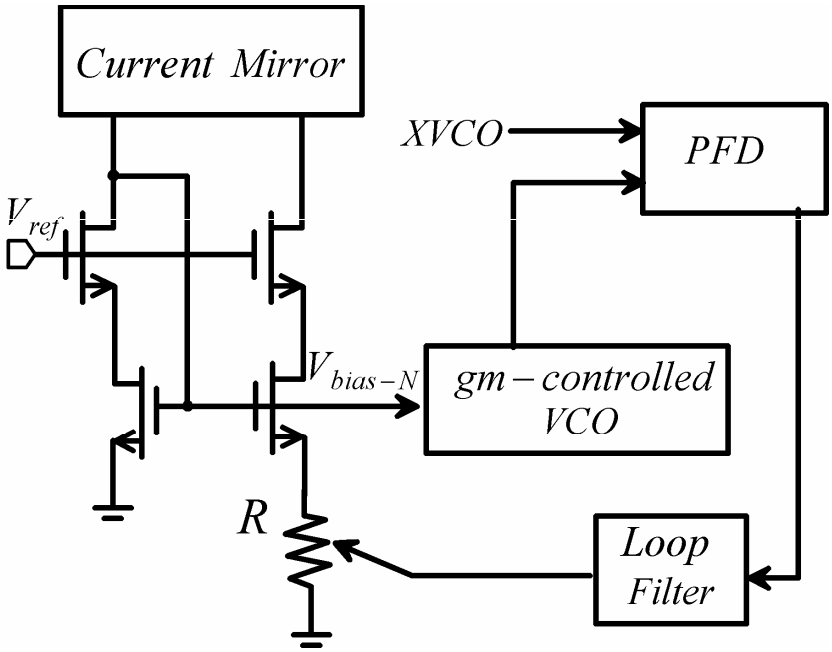


Figure 47: Constant-g_m biasing circuits for input OTA

The DC biasing part provides extra high-pass filtering to assist the overall low-frequency attenuation as the LC tank alone has a low-pass peaking response. Part 2 generates a fixed amount of G_m. Part 3 provides a small amount of continuously tuned G_m. It is meant to be small as the linearity is not as good as PDP. Part 4, 5, and 6 are the 3-bit digitally tuned G_m blocks. The W/L is tuned for linear G_m changes instead of the current.

To make sure that the G_m is invariant to the PVT variations, a constant-g_m biasing circuit [22] [34] is used as illustrated in Figure 47.

Between voltage controlled oscillator (VCO) and phase frequency detector (PFD), we can add an level shifter and an inverter to convert the differential-ended input to single-ended output with a sharp transition and a near 50% duty cycle. The circuit and simulation results are shown in Figure 48.

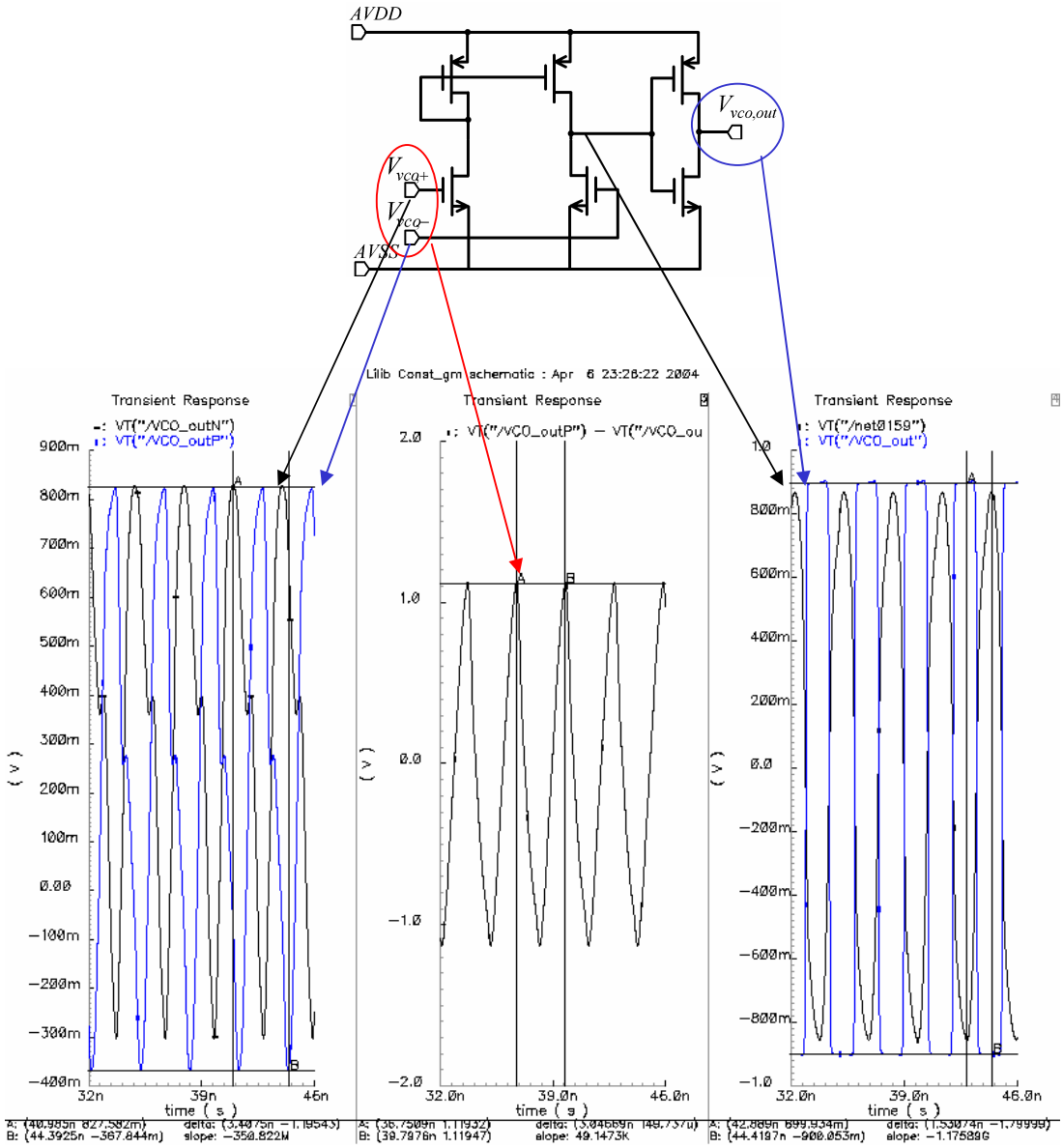


Figure 48: Level shifter + INV in constant-g_m biasing circuits

4.2.2 Tunable negative resistance design

The negative resistance circuit is shown in Figure 49. It is based on cross-coupled transistors. Part 1 generates a fixed amount of -g_m. Part 2 provides a small amount of continuously tuned -g_m. Part 3, 4, and 5 are the 3-bit digitally tuned -g_m blocks. Instead of using a level shifter [27], maximum overdrive is used to minimize its HD3. Also, if we tie the G/D of cross-coupled transistors to the LC tank terminals, the G/D capacitance can be absorbed into the tank enabling fastest speed. Again, the W/L is tuned for linear -g_m changes instead of the current.

4.2.3 Output buffer

The output buffer circuit is shown in Figure 50. It is based on the simple source follower. The design considerations are as follows:

1. It should match to 25Ω.
2. It should be biased to provide maximum output voltage swing.
3. It should be fast enough for the high frequency application.
4. It should have a separate power supply due to its large current consumption. So it will not disturb the other circuits.

Buffers effects on the circuit performance are summarized below.

1. Since it matches to 25 Ω transmission line connected to off-chip balun's differential side, the follower transistor generates an equivalent noise to 25 Ω resistor.
2. Noise from the biasing current source is directly added to output.
3. Source follower does introduce some distortion due to body effect and channel length modulation.
4. Source follower amplifies the noise from the filter due to a gain of less than 1.

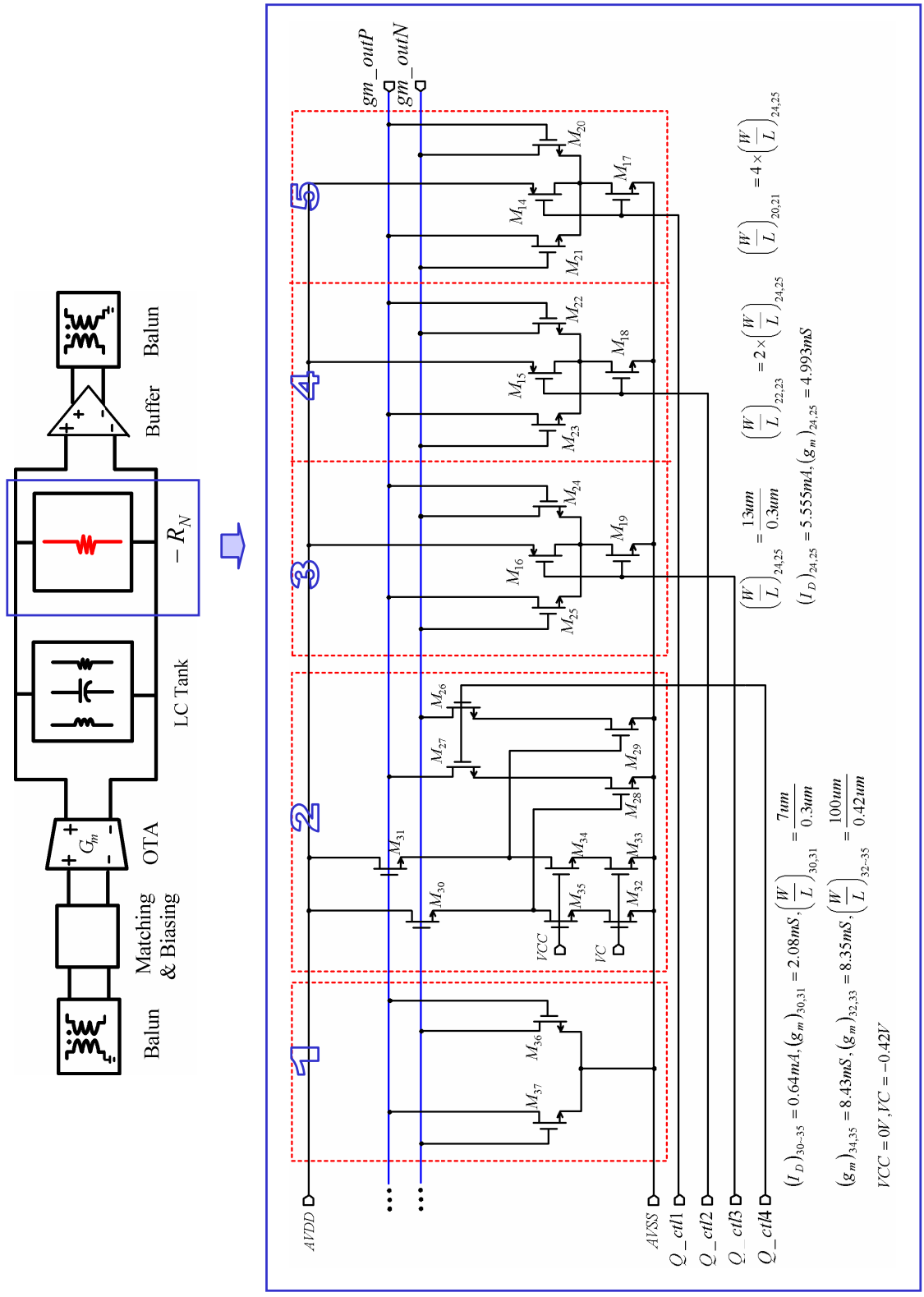


Figure 49: Tunable negative resistance for loss compensation (Parts 1-5 shown on figure).

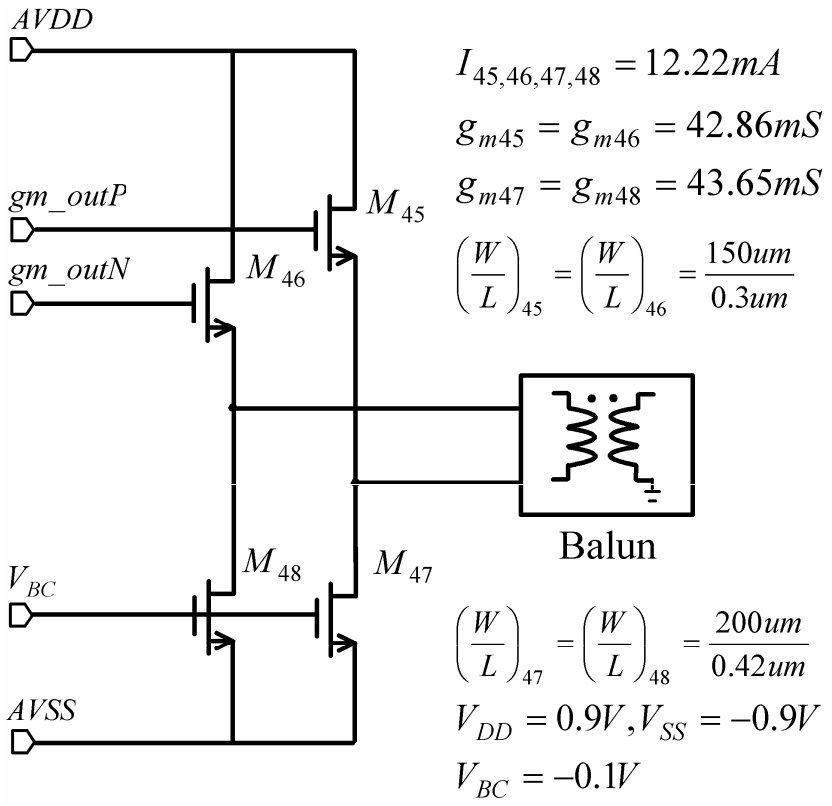


Figure 50: Output buffer.

Therefore, what we measure after this output buffer are conservative numbers for both linearity and noise performance of the filter itself.

4.3 Simulation results of one Q-enhanced LC tank BPF

Putting together all building blocks introduced in previous sections, we have the circuit for one Q-enhanced LC tank BPF that will be used in the Cadence simulation. For lucidity, only the core schematic is shown in Figure 51.

As explained in Section 4.1.1, the tank inductor can be simply modeled as a serial inductor and resistor. With the neutral point of the inductor connected to the power supply, we can get a voltage swing above AVDD, resulting a larger available linearity range. Also the inductor can provide some PSR. PSR can be improved further if

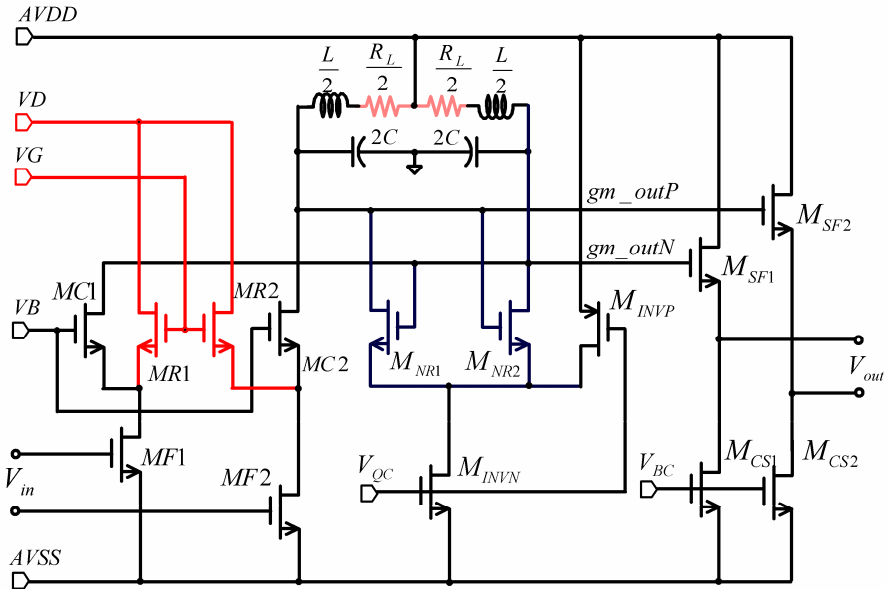


Figure 51: Core part of one Q-enhanced LC tank BPF.

the tank capacitor is connected in the way shown in Figure 51. As basically, if we look down from the power supply, the L and C form a ladder to short out the supply ripples. The loss compensation is implemented by a conventional cross-coupled negative resistor ($M_{NR1,2}$) switched in and out by the inverter ($M_{INVP,N}$) with a much stronger pull-down [27]. In this case, almost all supply voltage can be used to generate the negative resistance, resulting in better HD3 as the HD3 is inverse proportional to the applied overdrive squared. For a given inductance, smaller Q_0 means larger RL hence larger DC voltage drop, resulting in smaller overdrive voltage available to $M_{NR1,2}$, hence worse linearity. Also to achieve the desired Q, we need more negative resistance, hence more power and noise from negative resistor, which basically makes everything worse. Now suppose for a given Q_0, refer to Figure 37, if we pick the inductor k times larger, kL, then we will have kR_P, therefore more DC voltage drop and worse HD3. On the other hand, by observing

$$\frac{Q_0}{Q} = 1 - g_{mN} R_P \tag{45}$$

we will have g_{mN}/k, hence lower power and noise from negative resistance. However, the tank capacitor now becomes C/k. And due to kR_{PN} the input G_m will become G_m/k (hence lower power requirement from input OTA). To keep the gain constant, using (36) for thermal noise, we find that the thermal noise gets k times larger. Flicker noise will also be k times bigger due to k times smaller required sizes of G_m and g_{mN}. Therefore, we conclude that, for given Q_0, larger inductance results in lower power but higher noise performance and worse linearity. Other disadvantages of larger inductor are its lower SRF and lower Q_0. However making full use of the power supply to generate negative resistance does make it vulnerable to PVT variations. Consequently, it requires tuning circuitry.

In order to verify the synchronous tuning idea presented in Section 4.1.3 by simulation, the input OTA is replaced by the 3-bit PDP presented in Section 4.2.1; the negative resistor is replaced by the 3-bit negative resistance presented in Section 4.2.2; and the 3-bit TDC introduced in Section 3.2.3 is added in parallel with the tank C for f_0 shifting.

For the common digital cellular telephone and wireless data communication applications [43], the lowest frequency is about 900 MHz (GSM) and the highest frequency is about 5.775 GHz (HiperLAN/2). Therefore, two independent filters, one centered at the lowest frequency with 4nH inductor and the other centered at the highest frequency with 1nH inductor (both have an inductor Q of 5, assuming that either bulk substrate or SOI technology is available for simulation), are designed to verify the frequency handling capability of this design.

The AC simulation results for 5.775 GHz filter without and with synchronized tuning are shown in Figure 52. Figure 53 shows a more detailed plot of the AC response for 5.775 GHz filter with 3-bit synchronized tuning. Figure 54 shows the power, P1dB, input referred in-band noise, and 1 dB DR performance for 5.775 GHz filter with 3-bit synchronized tuning.

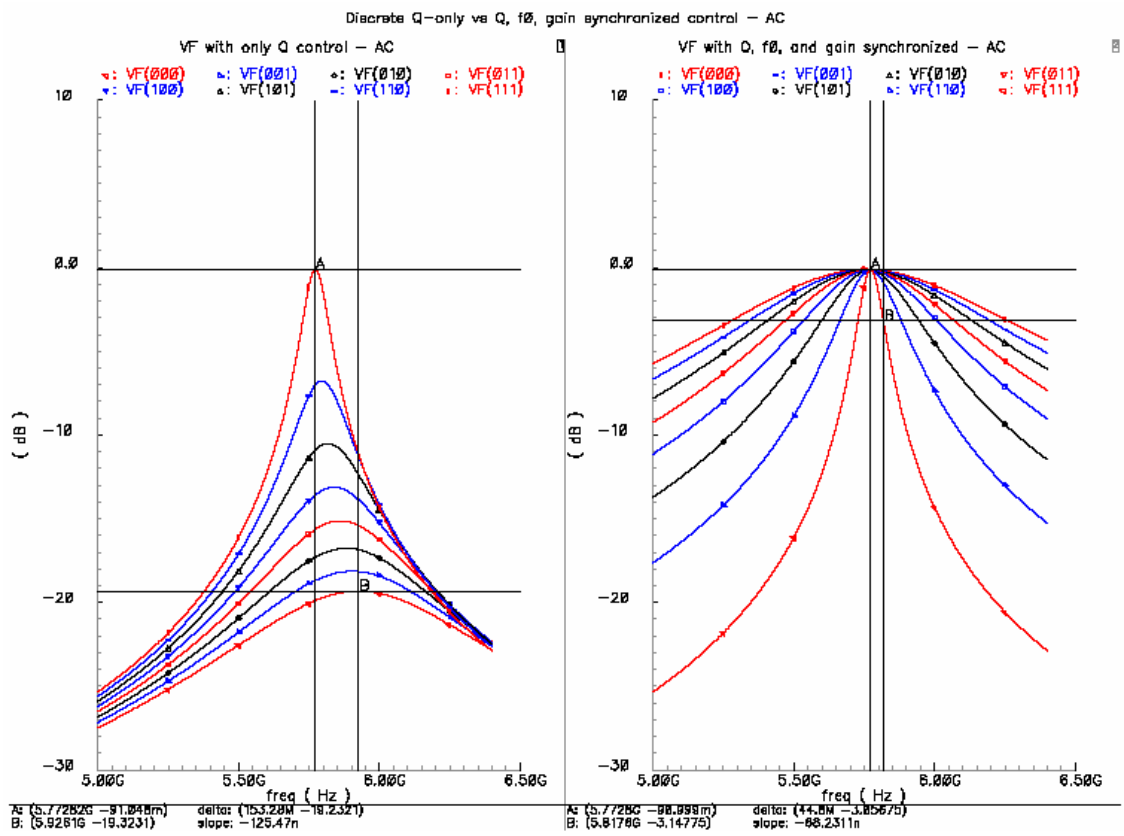


Figure 52: AC response for 5.775GHz filter without/with synchronized tuning.

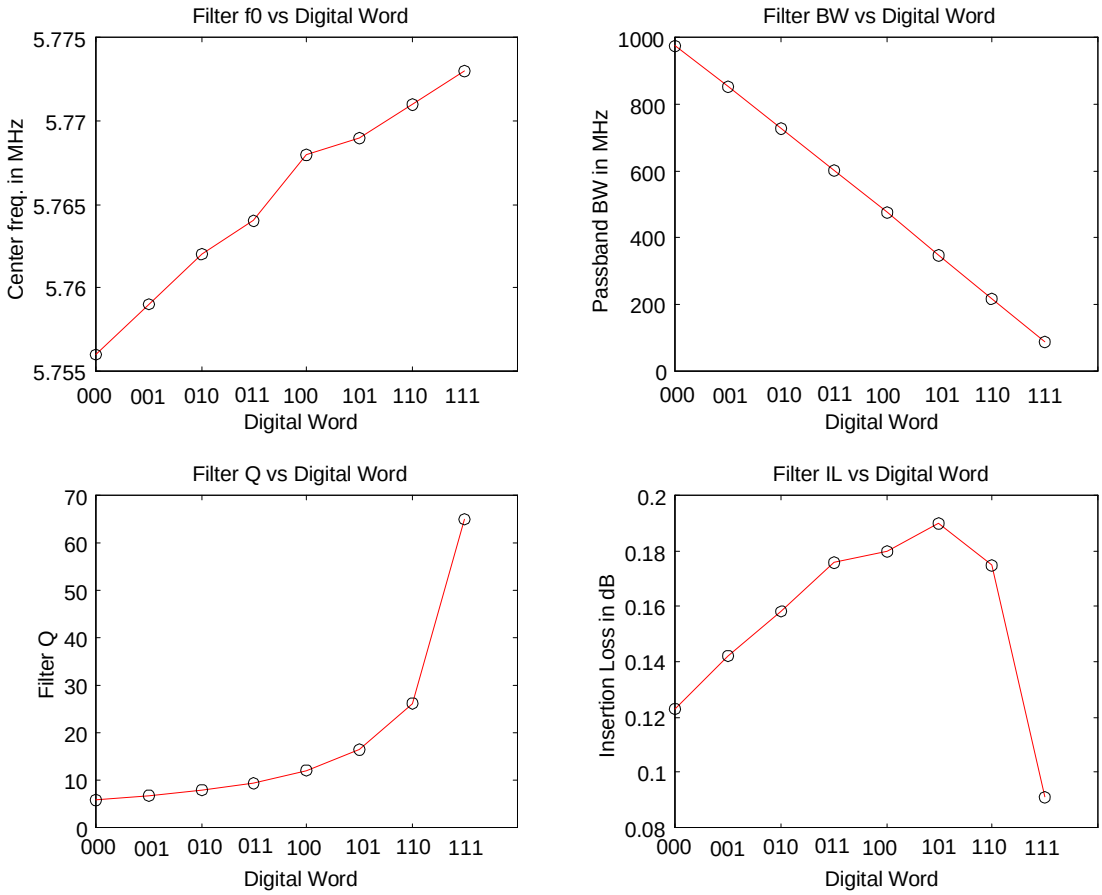


Figure 53: AC response for 5.775GHz filter with 3-bit synchronized tuning.

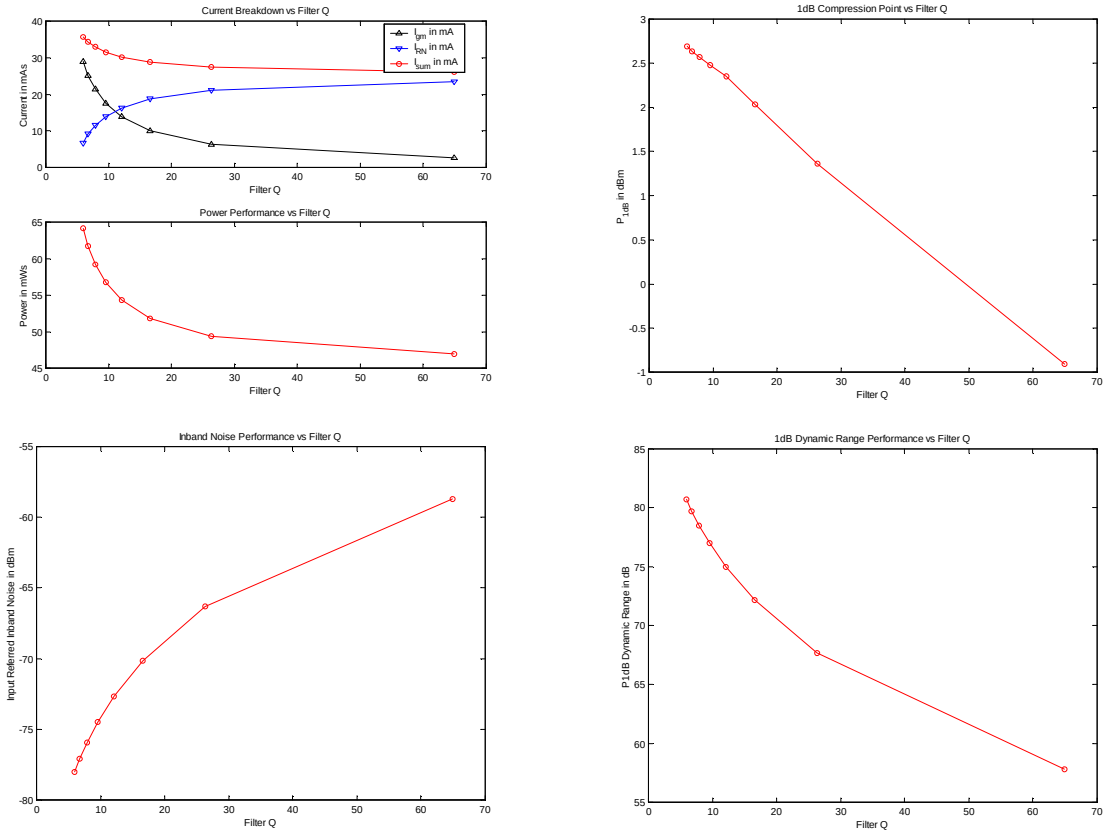


Figure 54: DR simulation for 5.775GHz filter with 3-bit synchronized tuning.

It can be seen from Figure 52 that without synchronized tuning, the gain varies by 19 dB and the center frequency varies by 154 MHz or ∼3%; while with synchronized tuning, the gain varies by 0.1 dB and the center frequency varies by 17 MHz or 0.3%. Similarly, for 900 MHz, without synchronized tuning, the gain varies by 18 dB and the center frequency varies by 16 MHz or ∼2%; while with synchronized tuning, the gain varies by 0.14 dB and the center frequency varies by 0.25 MHz or 0.03%. The detailed simulation results for 5.775 GHz BPF with synchronized tuning are listed in Table 8. The detailed simulation results for 900 MHz BPF with synchronized tuning are listed in Table 9.

4.4 Summary

In this chapter, we have first analyzed the one Q-enhanced LC tank BPF theoretically to provide some design guidelines. Based on these guidelines, we have then designed and explained the building blocks of the one Q-enhanced LC BPF. Two simulation cases have been presented to verify the proposed BPF's DR performance and frequency handling capability.

Table 8: Simulated performance of 5.775 GHz BPF with 3-bit synchronized tuning

Digital Word	111	110	101	100	011	010	001	000
f_0 **(GHz)**	5.773	5.771	5.769	5.768	5.764	5.762	5.759	5.756
BW (MHz)	88.9	219.3	348.48	476.29	603.4	728.34	852.6	975.1
Filter Q	64.9	26.32	16.55	12.11	9.55	7.91	6.75	5.9
I.L. (dB)	0.091	0.175	0.19	0.18	0.176	0.158	0.142	0.123
I_g_m **(mA)**	2.598	6.355	10.11	13.87	17.62	21.38	25.14	28.89
I_g_{mN} **(mA)**	23.48	21.08	18.69	16.3	13.91	11.53	9.145	6.765
I_sum **(mA)**	26.08	27.44	28.8	30.17	31.54	32.91	34.28	35.66
Power (mW)	46.94	49.39	51.84	54.3	56.77	59.24	61.71	64.19
P1dB (dBm)	-0.91	1.36	2.03	2.35	2.48	2.57	2.63	2.69
$\overline{v}_{in}^2$ **(dBm)**	-58.72	-66.31	-70.13	-72.65	-74.5	-75.93	-77.08	-78.03
P1dB DR (dB)[a]	57.81	67.67	72.16	75.00	76.98	78.50	79.71	80.72

[a]The above results are based on NSC 0.18 μm, low-VDD process with 1.8 V supply. Inductor of 1 nH with Q of 5, noise is integrated over 5.725-5.825 GHz.

Table 9: Simulated performance of 900 MHz BPF with 3-bit synchronized tuning

Digital Word	111	110	101	100	011	010	001	000
f_0 **(MHz)**	900	900	899.9	899.9	899.9	899.65	899.65	899.65
BW (MHz)	20.1	40.6	61.2	81.7	102.04	123.04	143.38	163.9
Filter Q	44.8	22.2	14.7	11.0	8.82	7.31	6.27	5.49
I.L. (dB)	0.23	0.14	0.108	0.085	0.073	0.058	0.046	0.034
I_g_m **(mA)**	2.42	4.95	7.48	10.01	12.54	15.07	17.61	20.14
I_g_{mN} **(mA)**	39.49	35.35	31.19	27.01	22.81	18.58	14.33	10.06
I_sum **(mA)**	41.91	40.3	38.67	37.02	35.35	33.66	31.94	30.2
Power (mW)	75.43	72.54	69.61	66.64	63.63	60.58	57.49	54.36
P1dB (dBm)	8.22	8.93	9.13	9.19	9.3	9.31	9.36	9.36
$\overline{v}_{in}^2$ **(dBm)**	-61.65	-68.02	-71.76	-74.45	-76.57	-78.32	-78.82	-81.15
P1dB DR (dB)[a]	69.87	76.95	80.89	83.64	85.87	87.63	89.18	90.5

[a]The above results are based on NSC 0.18 μm, low-VDD process with 1.8 V supply. Inductor of 4 nH with Q of 5, noise is integrated over 890-910 MHz.

CHAPTER 5

PROTOTYPE DESIGN AND MEASUREMENT RESULTS

In order to verify the linearity-enhancement techniques illustrated in previous chapters, a simplified one Q-enhanced LC tank BPF is fabricated. The circuit implementations in the prototype design are described in Section 5.1. The measurement results are presented in Section 5.2.

5.1 Prototype design

To increase the chance of first run success and demonstrate the most important research results, a simplified one Q-enhanced LC tank BPF is implemented and fabricated. The tape-out BPF design is explained as follows.

To enhance the Q and save some area, the LC tank inductor is implemented as an octagonal, differential structure, with top metal only inductor without center ground shield. The center neutral point of the inductor is tied to the power supply (VDD). The layout of tank L is shown in Figure 55.

The LC tank capacitor is implemented by a parallel combination of two poly-poly capacitors with their top and bottom plates flipped as shown in Figure 56. In this way, the total capacitances at each terminal are balanced. In order to achieve the best matching of these two capacitors, each capacitor has been equally divided into 8 unit square elements, which are connected in the way shown in Figure 56 using common-centroid and high-dispersion techniques. All the top plates are used for wiring to reduce the interconnection losses hence to improve the Q. As shown in Figure 57, the tank capacitors are surrounded by the dummy capacitors to reduce the etching effect

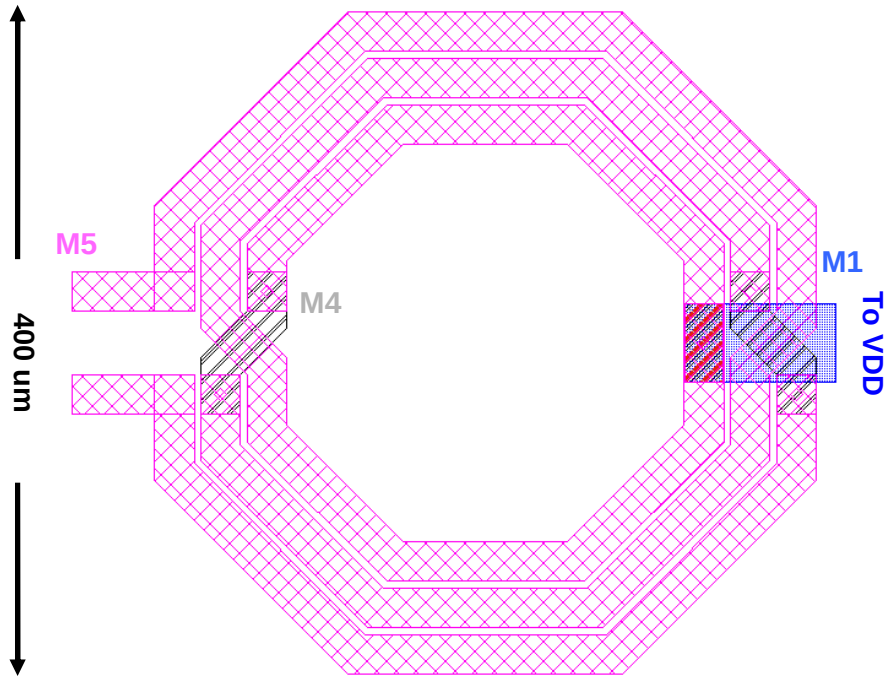


Figure 55: Layout of tank L.

of each unit element. To reduce the coupling with the other part of the circuit, all the capacitors are put on top of two n-WELLs that are biased at VDD. All the dummy capacitors are also tied to VDD to reduce their capacitive coupling with the tank C.

The tunable PDP illustrated in Section 4.2.1 is used for the input OTA with layout shown in Figure 58. The layout for the 2× PDP cell shown in the red box in Figure 58 is zoomed in as shown Figure 59. The poly-resistor and poly-capacitor are used for the DC biasing and block part. Constant-g_m biasing circuitry is not included in the prototype design in order to reduce the complexity. A 50 Ω poly-resistor is used for input matching. The tunable negative resistance design presented in Section 4.2.2 is used for the loss compensation with layout shown in Figure 60. The layout for the 1× negative resistance cell shown in the red box in Figure 60 is zoomed in as shown in Figure 61. The output buffer used is the one explained in Section 4.2.3.

The circuit is fabricated with NSC's 0.18 μm epi-substrate 2P5M process. The

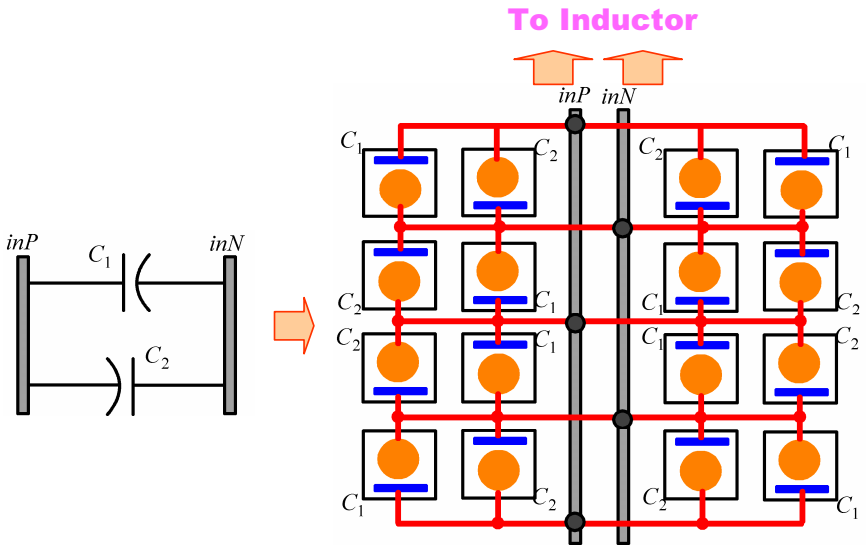


Figure 56: Configuration of tank C.

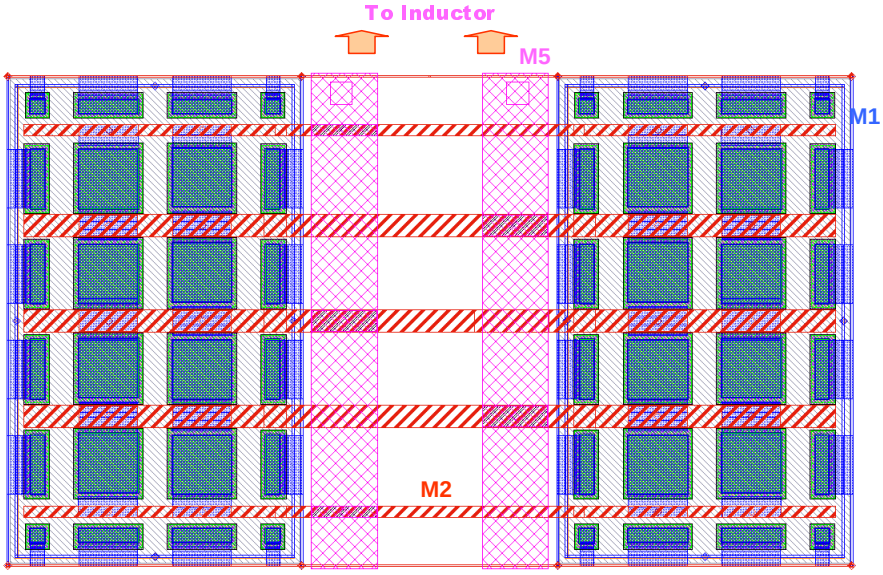


Figure 57: Layout of tank C.

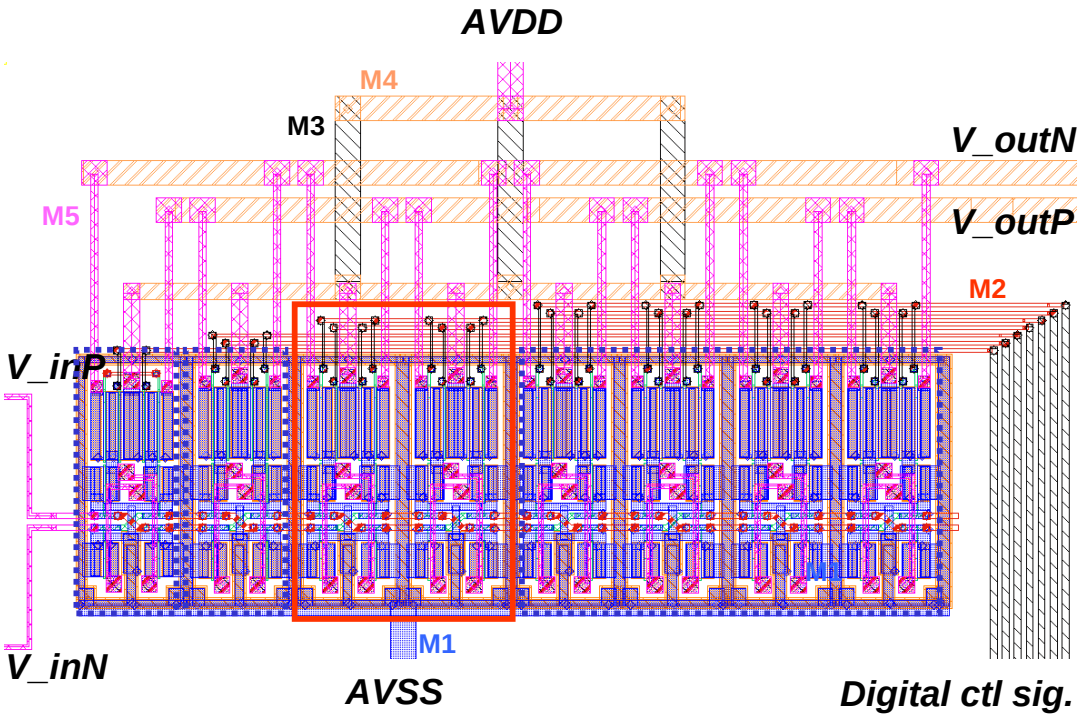


Figure 58: Layout of input OTA.

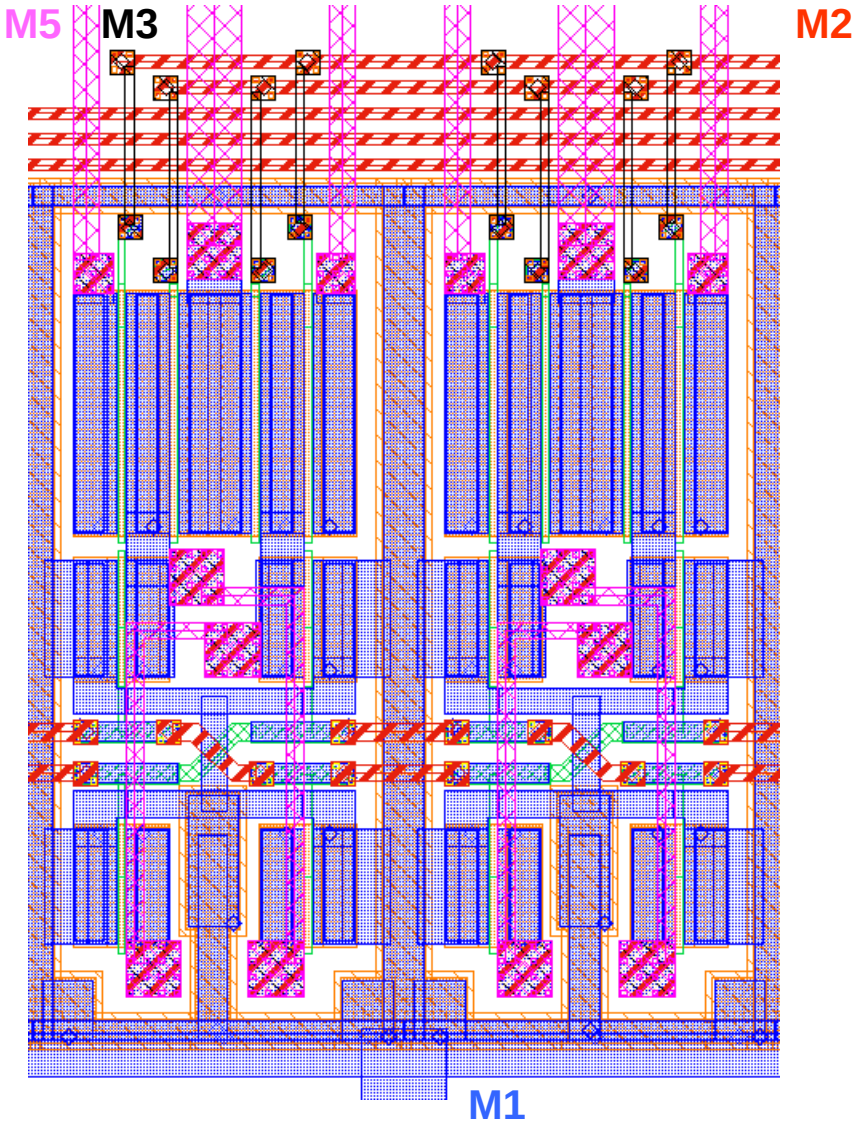


Figure 59: A layout zoom-in for the 2× PDP cell.

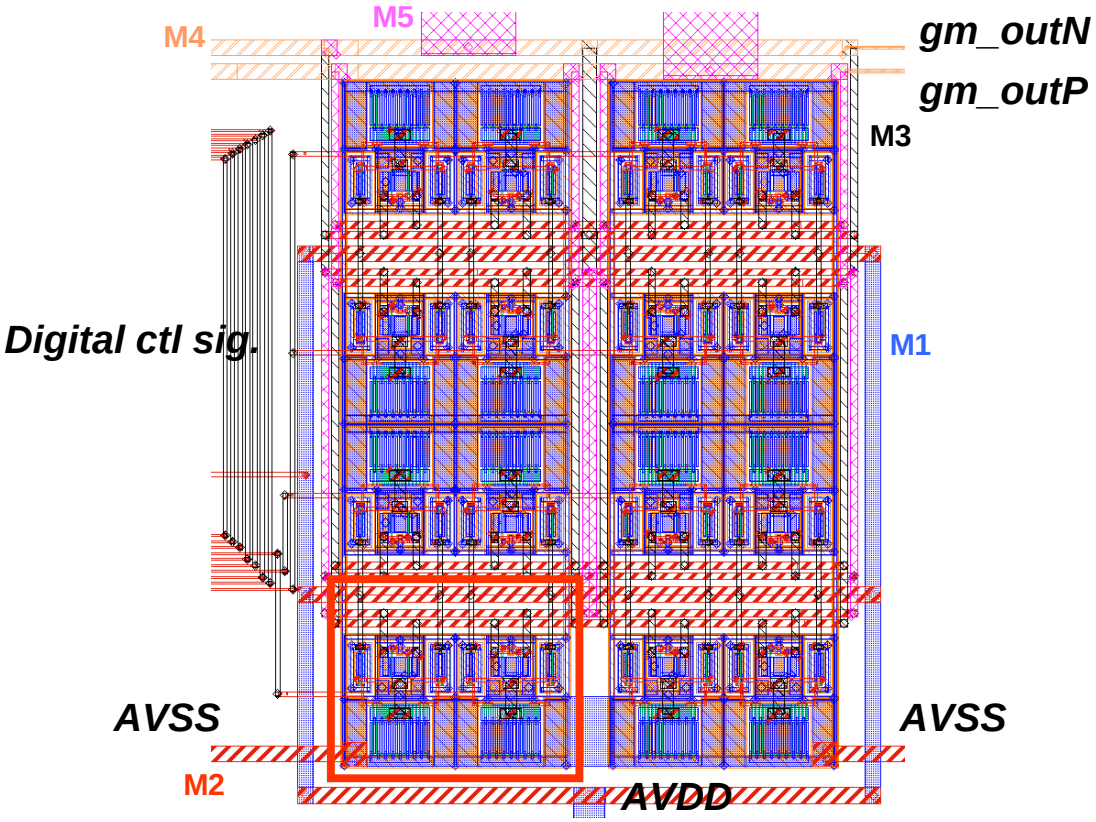


Figure 60: Layout of negative resistor.

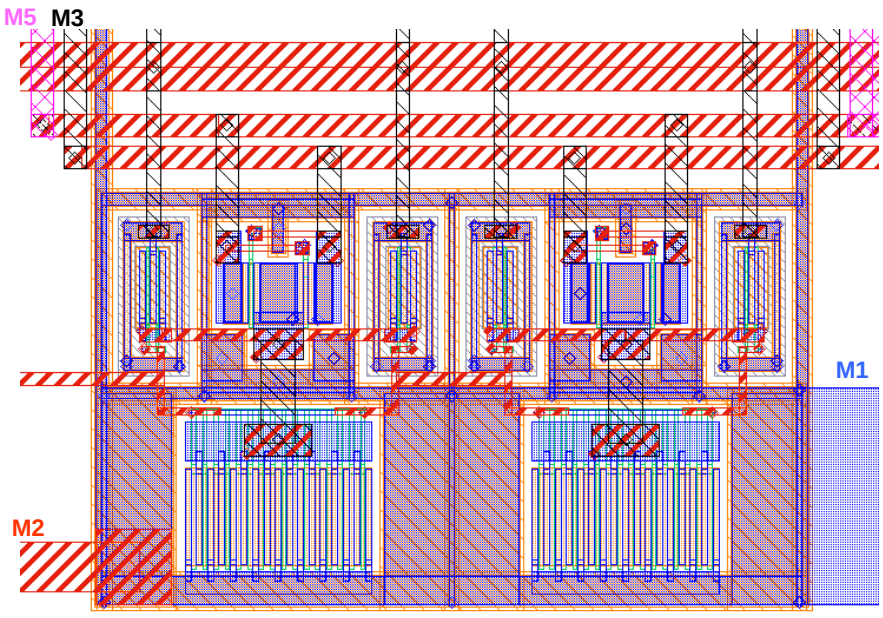


Figure 61: A layout zoom-in for the 1× PDP cell.

chip microphotograph is shown in Figure 62. It measures about $1.21mm \times 1.45mm$. A Leadless Lead-frame type Package (LLP) with 28 pins from NSC is picked for its excellent frequency capability, thermal performance, and small footprint. Figure 63 shows the bonding diagram used for this design. The packaged chip is then put on an ad-hoc designed printed circuit board (PCB) with some rework tool followed by an 8-step reflow. Off-chip baluns are used for single-ended to differential-ended signal conversions. These baluns and PCB traces introduce some loss that has been de-embedded in the following measurements. Once the measurements are done, some k-shell and perl scripts are used to read out the data through HPIB interface. The measured data are then plotted out. These scripts can also be used for measurement automation.

The schematic for PCB assembly is shown in Figure 64. The bill of material (BOM) used to build the PCB is shown in Table 10.

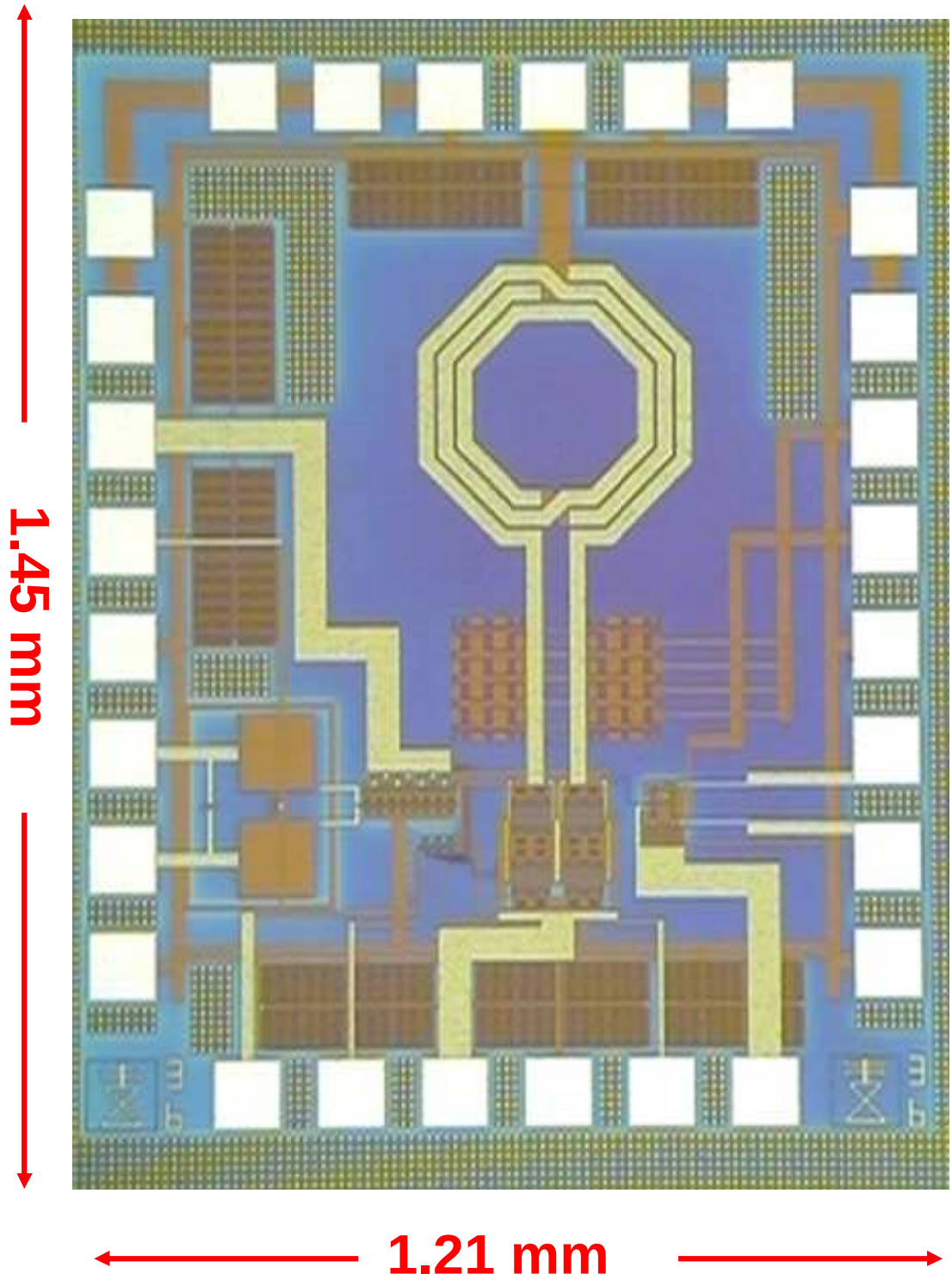


Figure 62: Chip microphotograph.

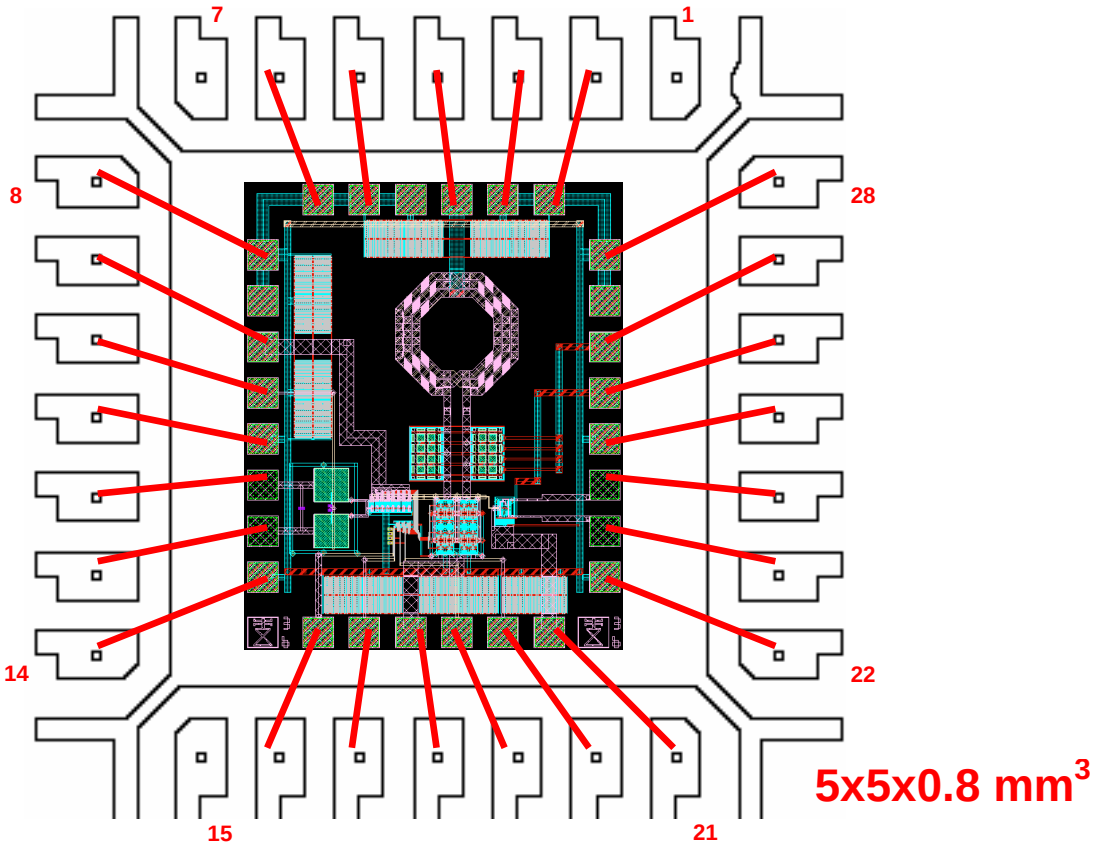


Figure 63: Bonding diagraph for LLP-28 package request.

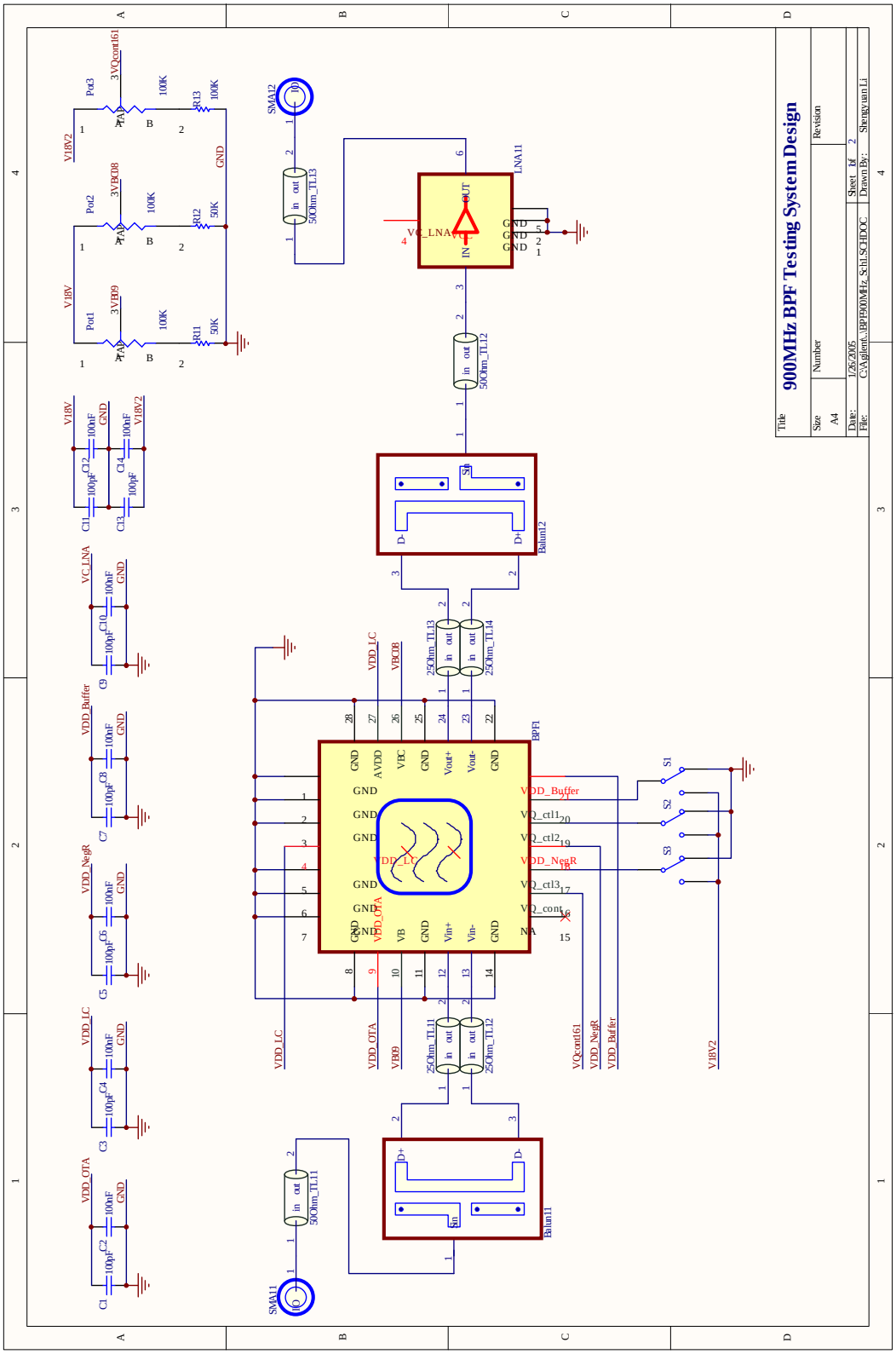


Figure 64: PCB schematic.

Table 10: Bill of material for PCB

Quantity	Part Number	Comments
1	RHM100KCCT-ND (Digi-Key)	100 KΩ resistors for biasing voltage setting
2	RHM49.9KCCT-ND (Digi-Key)	49.9 KΩ resistors for biasing voltage setting
4	RHM49.9CCT-ND (Digi-Key)	49.9 Ω resistors for 25 Ω load calibration in SOLT
3	D4AA15-ND (Digi-Key)	100 KΩ Potentiometers for biasing voltage setting
7	490-1615-1-ND (Digi-Key)	100 pF ceramic capacitors for power bypassing
7	490-1666-1-ND (Digi-Key)	100 nF ceramic capacitors for power bypassing
10	J502-ND (Digi-Key)	SMA-50 edge-mounted connectors for RF signal I/O
10	Anaren 3A425	*Xingle*® Balun for diff-end and single-ended signal conversions
12	J147-ND (Digi-Key)	Banana Jacks for DC power supplies
3	360-1012-ND (Digi-Key)	SPDT toggle switches for digital control

5.2 Measurement results

The frequency response is measured by a synchronized tracking generator and spectrum analyzer. The measured frequency response is shown in Figure 65. It peaks around 844.9 MHz with a filter Q of about 16.7 (for which we call low-Q case) and the 3 dB BW of about 50.6 MHz. The insertion loss is measured to be 4 dB after deducting the losses from other parts such as off-chip baluns, PCB trances etc with a through de-embedding structure.

Since the noise floor of the spectrum analyzer used is about -141 dBm/Hz (well above the filter's noise floor), a pre-amp with 24 dBm gain is used in order to measure the filter's output noise PSD. 0dB attenuation in spectrum analyzer is used to avoid any unwanted internal noise amplification and the power gain and NF of the pre-amp

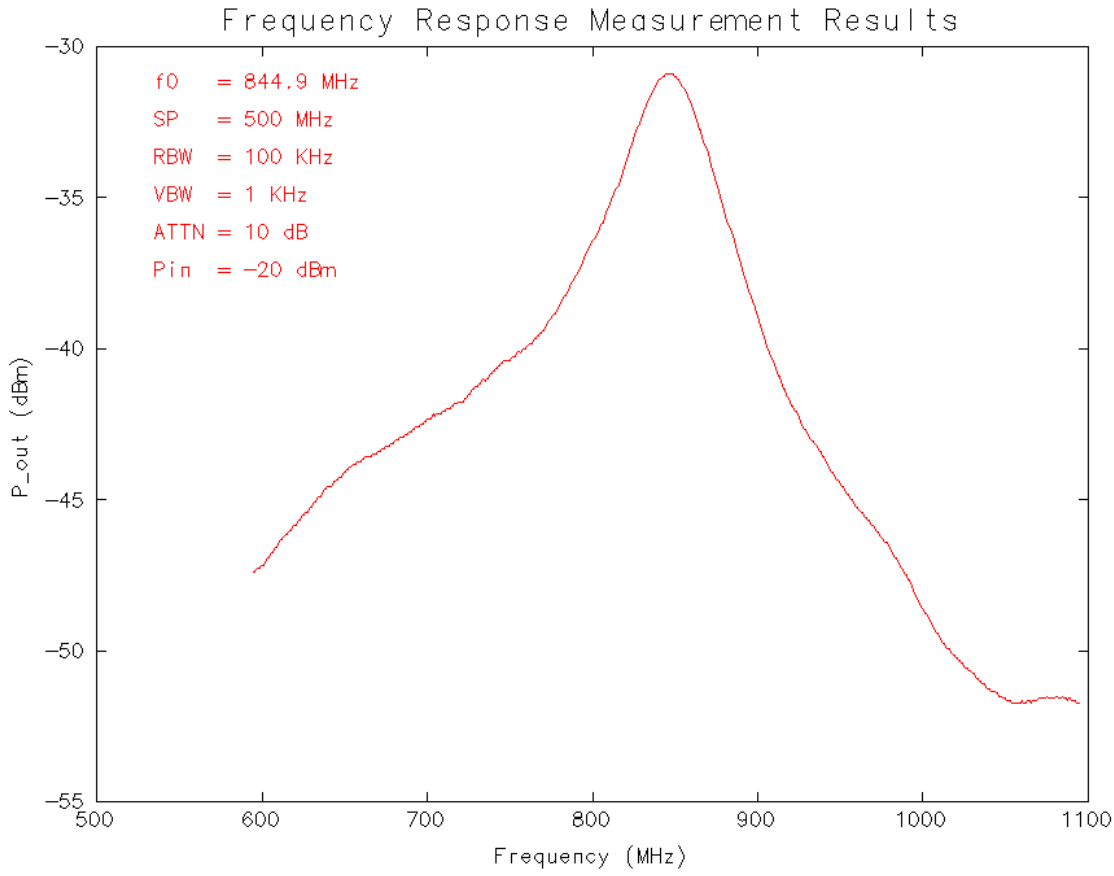


Figure 65: Measured frequency response (low-Q case).

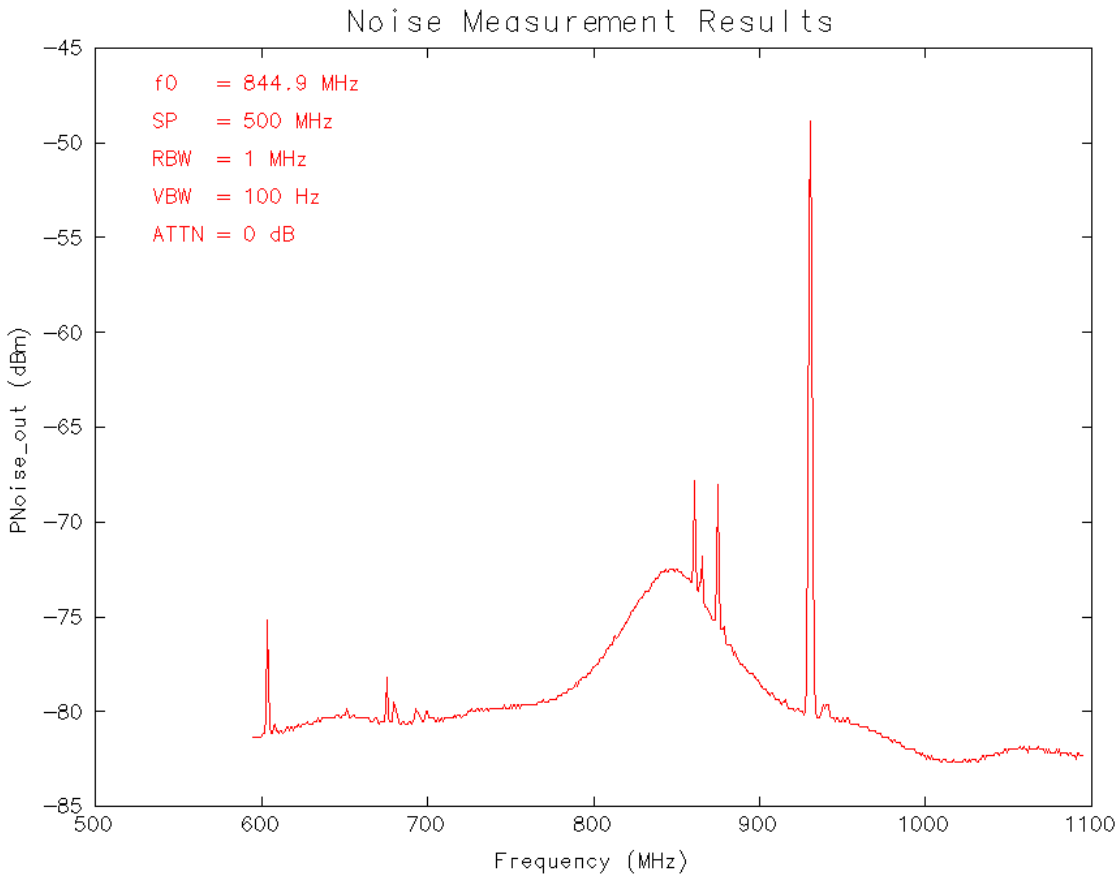


Figure 66: Measured output noise PSD with pre-Amp (low-Q case).

is also measured and de-embedded using simple gain method. The PSD without pre-amp de-embedding is shown in Figure 66. It basically follows the filter shape as we expect.

For linearity, the 1dB compression point is measured through one-tone test at center frequency. An RF signal generator is used to generate the fixed peaking center frequency input signal with varied amplitude and the output is monitored by the spectrum analyzer. The 1dB compression point is the input amplitude where the output gain drops by 1 dB. The off-chip balun's linearity is measured via a through test structure and it is verified that the distortion from balun at the above measurement data points is negligible. The measured data are plotted in Figure 67. And P1dB is extrapolated to be +4 dBm.

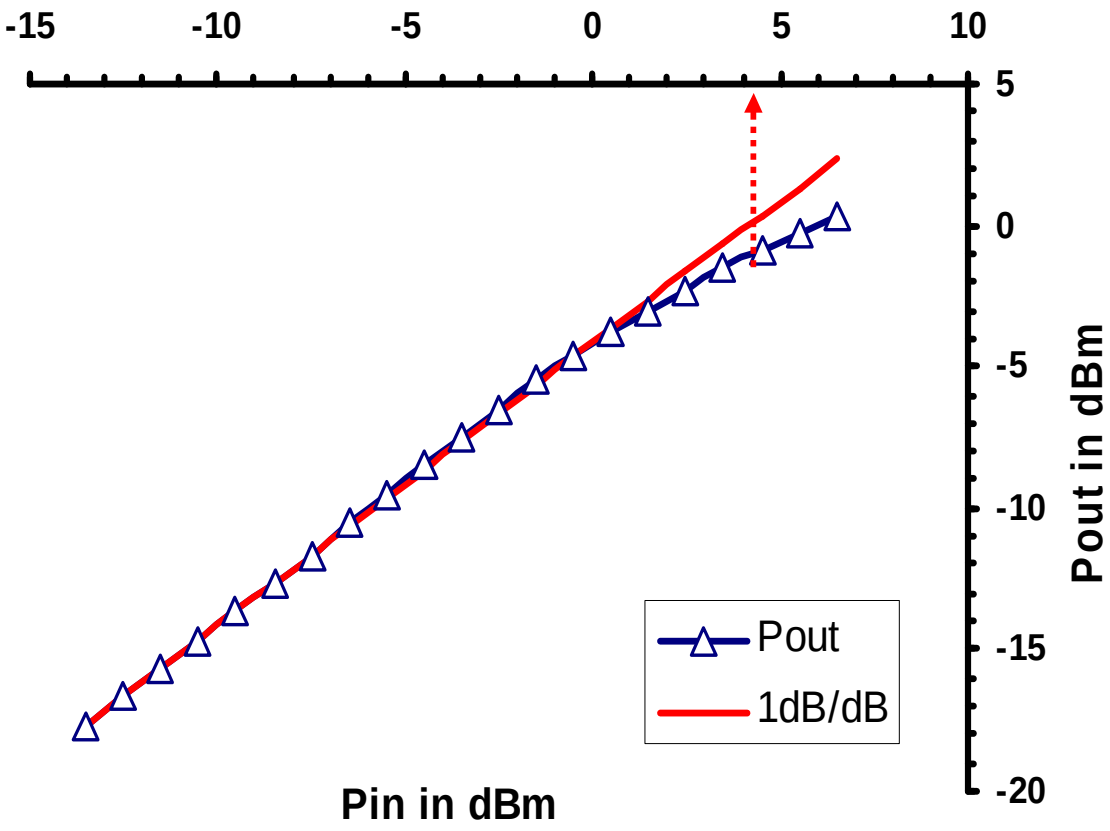


Figure 67: P1dB measurement results (low-Q case).

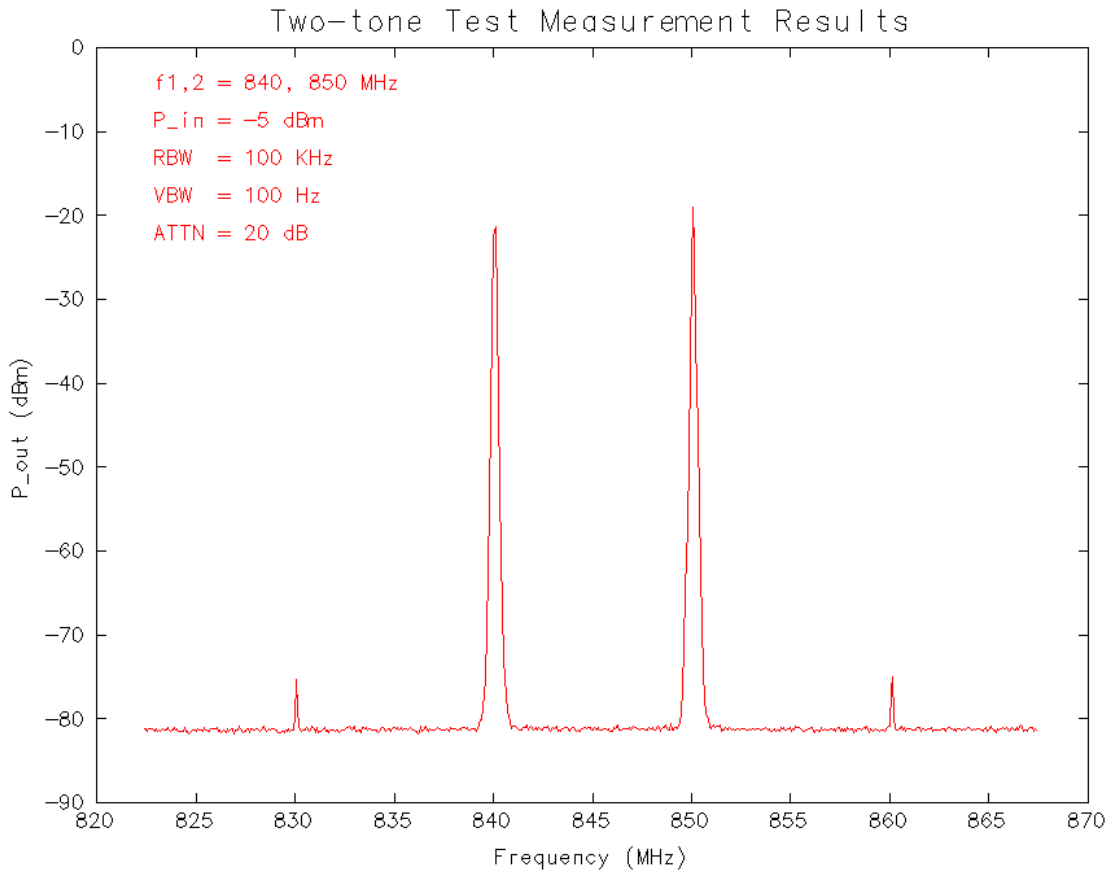


Figure 68: Measured two-tone test spectrum (low-Q case).

Figure 68 shows the two-tone test measured spectrum. With two frequencies at 840 and 850MHz, IIP3 is extrapolated to be +16 dBm shown in Figure 69. Note the extrapolations for both P1dB and IIP3 are done with all the loss up to the filter chip input and output ports de-embedded. Also, care is taken in adjusting the attenuation levels of spectrum analyzer in order not to saturate the internal mixer.

By switching more negative resistance, a filter Q of about 70.5 (for which we call high-Q case) peaking at 845.6 MHz can be obtained. The P1dB and IIP3 points can be extrapolated from the measured one-tone and two-tone test data shown in Figure 70 and Figure 71 respectively.

The measurement results for both low-Q case and high-Q case are summarized in Table 11. The equipment used in the measurement are listed in Table 12.

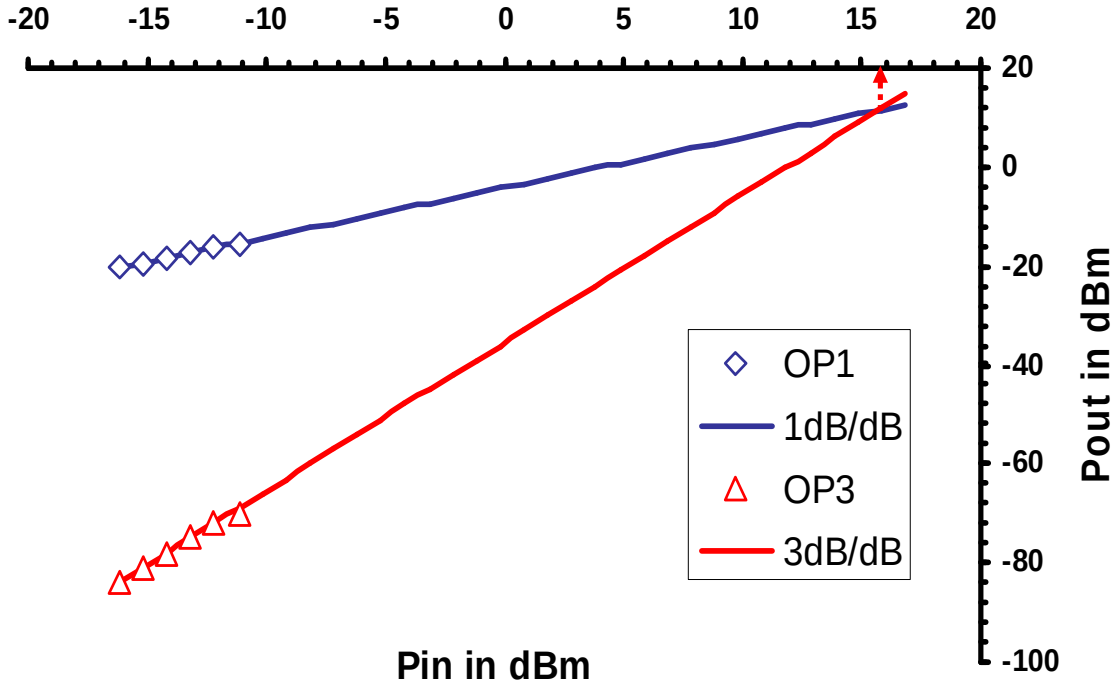


Figure 69: IIP3 measurement results (low-Q case).

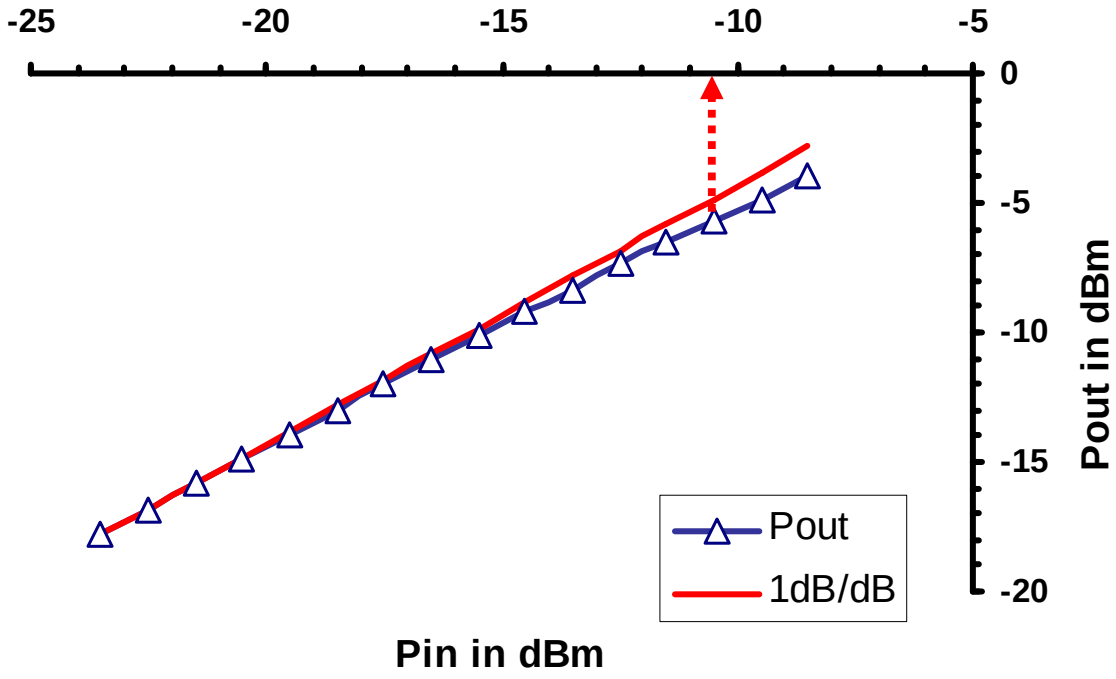


Figure 70: P1dB measurement results (high-Q case).

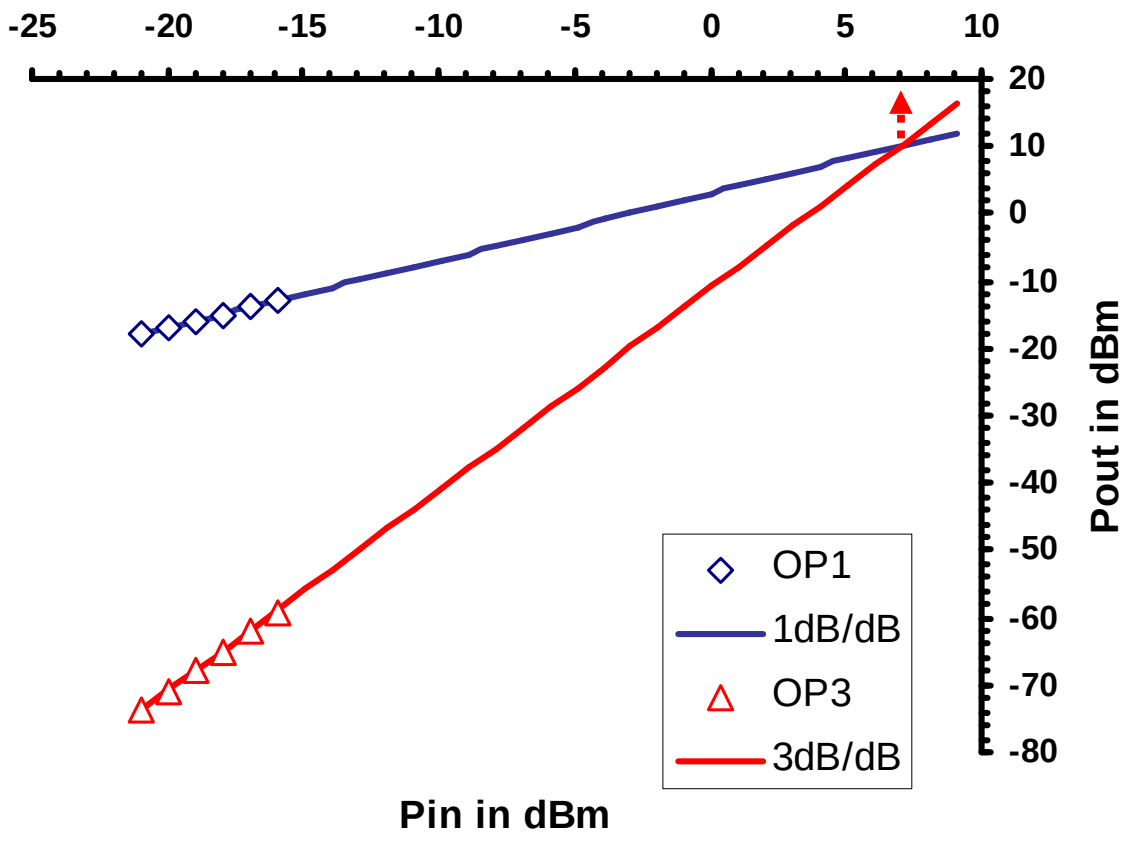


Figure 71: IIP3 measurement results (high-Q case).

Table 11: Measured performance

Process	NSC 0.18 μm CMOS9 2P5M	
Supply Voltage	1.8 V	
Area	1.75 mm^2	
Center Frequency	844.9 MHz	845.6 MHz
BW/f_{-3dB}/f_{+3dB}	50.6 MHz/25.3 MHz/25.3 MHz	12 MHz/6 MHz/6 MHz
Filter Q	16.7 (low-Q case)	70.5 (high-Q case)
Insertion Loss	4 dB	-5.67 dB
Max. Output Noise PSD	-157 dBm/Hz	-147 dBm/Hz
Total in-band Noise	-84 dBm [a]	-74 dBm [b]
P1dB	+4 dBm	-9.5 dBm
IIP3	+16 dBm	+7 dBm
P1dB DR	88 dB	65 dB
SFDR [c]	71 dB	57 dB
Supply Current	56.7 mA	60.4 mA
Inductor Q	$\sim$1 at center frequency	

[a] based on Max. P_{no} PSD and 20MHz BW
[b] based on Max. P_{no} PSD and 20MHz BW
[c] over 20MHz BW

5.3 Summary

In this chapter, we have first presented the prototype design for the one Q-enhanced LC tank BPF with layout, packaging request, and PCB design information. DC, frequency response, noise, one tone test, and two tone test measurement results are then presented for the tape-out BPF.

Table 12: A list of equipment used in measurement

Equipment	**Model**	**Comments**
Spectrum Analyzer (×1)	Agilent 8563E	Scalar spectrum display (30 Hz - 26.5 GHz)
RF Tracking Generator (×1)	HP 85640A	Frequency sweeping (300 KHz - 2.9 GHz, DR greater than 100 when combined with Spectrum Analyzer)
DC block capacitor (×2)	Picosecond 5501A, 5508	DC block for DC coupled only Spectrum Analyzer and Track Generator 5501A: 7 KHz to >26 GHz, 0.22 uF with 10 ps risetime 5508: 0.7 KHz to >26 GHz, 2.2 μF with 8 ps risetime
LNA/Pre-Amp (×1)	HP 87405A	10 - 3000 MHz, 24 dB gain, NF of 6.5, +13 dBm max input for noise measurement
Power Supply (×3)	HP E3631A	DC power supply (6 V with upto 5 A current output)
Multimeter (×3)	HP 34401A	Current monitoring (with resolution upto 10 nA on 10 mA range)
RF signal generator (×2)	HP 8656B, HP 8662A	One-tone and Two-tone test HP 8656B Signal Generator: 0.1 - 990 MHz HP 8662A synthesized Signal Generator: 10 KHz - 1280 MHz
Hybrid (×1)	Anaren 30054	Power Combining for two-tone test (0.5 - 1.0 GHz)
VNA (×1)	HP 8510	s-parameter measurement
RF cables (×4)	NA	Equipment connections
SMA, BNC, type-N Converters	NA	Connector conversions
50 Ω load with SMA connector	NA	Input termination for noise measurement and hybrid difference port termination for two-tone test
Bias Tee	HP 11612A	Bias Network (45 MHz - 26.5 GHz, 40 VDC, 0.5 A MAX, 50 Ω)

CHAPTER 6

CONCLUSIONS

6.1 Summary

A 845 MHz RF filter using one Q-enhanced LC tank is designed and fabricated with NSC's standard 0.18 μm digital epi–substrate CMOS technology. The measurement results show that with filter Q of 17 at 845 MHz, the 1 dB compression point is +4 dBm, IIP3 to be +16 dBm with a peak noise floor of -154 dBm/Hz, and SFDR to be 71. With filter Q of 70 over 20 MHz BW, the 1 dB compression point is measured to be -9.5 dBm, IIP3 is +7 dBm with a peak noise floor of -141 dBm/Hz, and SFDR is 57 over 20 MHz BW. With a power supply of 1.8 V, it uses 56 mA for low-Q case and 60 mA for high-Q case due to the low-Q (Q$\sim$1) of inductor.

As a reference, the measurement results (Low-Q Case and High-Q Case) are compared with those of other RF filters published recently. As we can see from Table 13, the proposed RF filter achieves the highest DR so far even with an inductor Q$\sim$1. The DR can be even higher if inductor Q can be improved as DR is proportional to Q^2. The high DR achieved is attributed to the new PDP design and the idea of maximizing the overdrive of the input OTA and negative resistance.

6.2 Future work

After the core RF filter using one Q-enhanced LC tank has been demonstrated to work with an excellent DR, the future work could focus on the actual implementation of the proposed RF filter on-chip. Specifically, the following needs to be done:

1. The constant-g_m biasing circuitry needs to be demonstrated to ensure that the input OTA is process, voltage, and temperature stable.

Table 13: Measured performance comparison

	Chet [49]	**Li [30]**	**Dulger [13]**	**Mohieldin [37]**	**Kuhn [27]**	**Low-Q Case**	**High-Q Case**
P1dB DR	64	65	38	42	63	**88 dB**	**65 dB**
P1dB/IIP3	-13.4/-4.9 dBm	-9.5/0 dBm	-30/-17.5 dBm	-26/-14 dBm	-5.5/0 dBm	**+4/+16 dBm**	**-9.5/+7 dBm**
Max. output noise PSD	-155 dBm/Hz	-156 dBm/Hz	-152 dBm/Hz	-137 dBm/Hz	-142 dBm/Hz	-157 dBm/Hz	-147 dBm/Hz
f0	2.14 GHz	1.88 GHz	2.19 GHz	1.84 GHz	900 MHz	844.9 MHz	845.6 MHz
BW	60 MHz	150 MHz	53.8 MHz	80 MHz	20 MHz	50.6 MHz	12 MHz
Filter Q	35.7	12.5	40.7	23	45	16.7	70.5
I.L.	0 dB	2 dB	5 dB	-9 dB	-11 dB	4 dB	-5.67 dB
Power	7 mA	18 mA	4 mA	16 mA	13 mA	56.7 mA	60.4 mA
VDD	2.5 V	3 V	1.3 V	2.7 V	3.0 V	1.8 V	
Tech.	0.25 μm CMOS bulk-sub.	0.25 μm BiCMOS bulk-sub.	0.35 μm CMOS epi-sub.	0.5 μm CMOS epi-sub.	0.5 μm SOS	0.18 μm CMOS epi-sub.	
Inductor Q	$\sim$5(4.3nH)	>12(4nH)	2(3.7nH)	2.7(3nH)	>8(16nH)	**$\sim$1(4nH)**	

2. The new proposed two-level inductor needs to be demonstrated to ensure the wide frequency tuning capability of the BPF.

3. The new proposed wide-range tunable linear varactor needs to be demonstrated to ensure good frequency tunability while maintaining good linearity.

4. The automatic tuning circuitry needs to be designed and demonstrated to be able to tune the gain, center frequency, and filter Q within certain tolerance in a certain amount of time.

6.3 Research contributions

The research contributions from this work are listed below:

1. A new simple pseudo-differential pair (PDP) for input g_m stage design. It is the fastest high-linearity, low-distortion, wide-range, and constant–g_m design reported to date. This has been applied in the final filter tap-out and proven experimentally.

2. A new tunable discrete inductor (TDL) design to achieve two-level inductance with the same real estate that can be used to expand the filtering frequency range. This has been verified experimentally.

3. A new tunable discrete capacitor (TDC) design to achieve high linearity over wide terminal voltage swing range. This has been verified through simulation.

4. The design of a Q-enhanced LC filter in a new systematic way to achieve synchronized gain, center frequency, and filter Q tuning capability. This has been verified through simulation.

The fabricated 900 MHz filter, with NSC's standard 0.18 μm digital epi–substrate CMOS technology, achieves the highest DR so far even with an inductor Q of just

around 1 compared with a typical value > 8 in the previous published work. Two ISCAS papers [31][32] have been generated directly from this work.

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VITA

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He came to Georgia Institute of Technology in Fall 2000 and earned his Master of Science in Digital Signal Processing (DSP) from school of ECE in 2001. In Spring 2002, he started learning his first modern IC design courses (ECE6412, 6414, and 6435) while teaching-assisting ECE3042. He then joined Dr. Phillip E. Allen's Analog IC Design Group in Fall 2002. In that sense, he claims himself as an IC designer purely made in Tech. His PhD thesis mainly results from an RF filter project funded by Agilent Labs at Palo Alto, CA starting from Spring 2004. Most of the measurement results are also obtained at Agilent Labs while he was hired as an technical Intern there from March to May 2005.

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